FIG. 1A

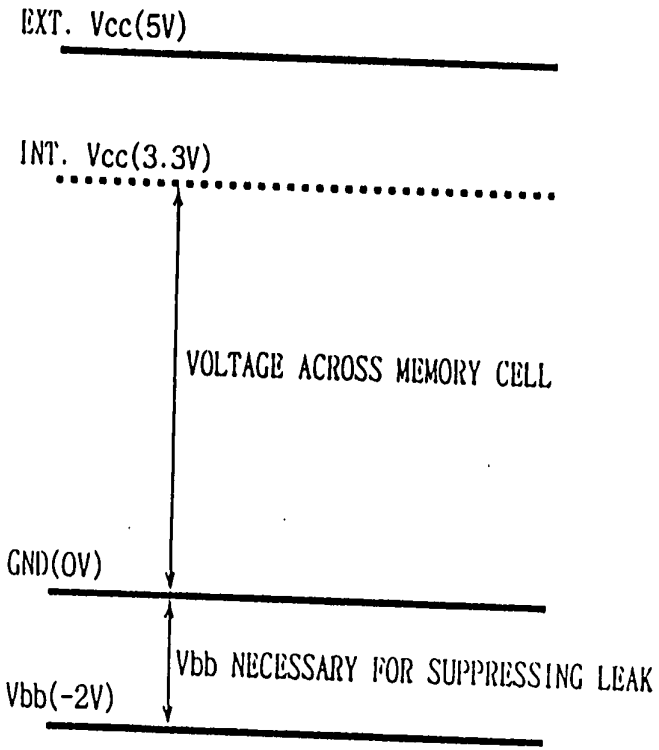

EXT. Vcc(5V)
INT. Vcc(3.3V)
VOLTAGE ACROSS MEMORY CELL
GND(0V)
Vbb NECESSARY FOR SUPPRESSING LEAK
Vbb(-2V)

FIG. 1B

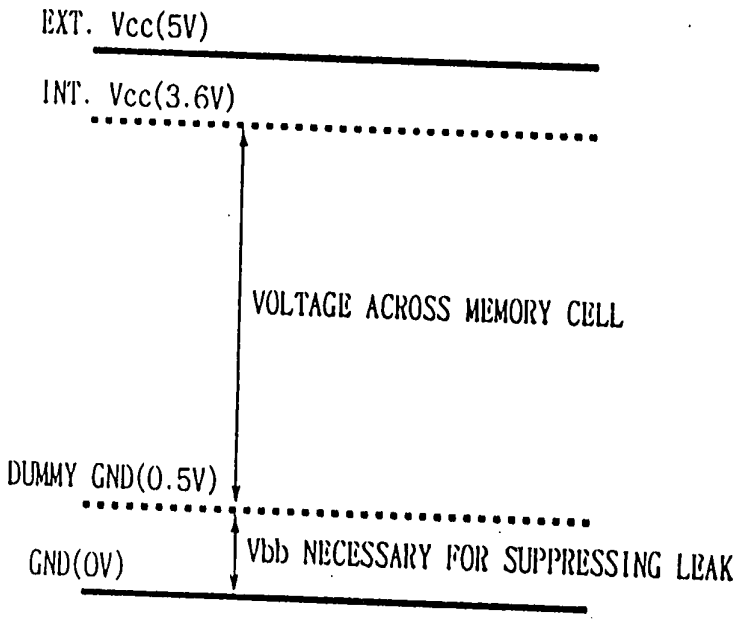

EXT. Vcc(5V)
INT. Vcc(3.6V)
VOLTAGE ACROSS MEMORY CELL
DUMMY GND(0.5V)
GND(0V)
Vbb NECESSARY FOR SUPPRESSING LEAK

FIG. 2

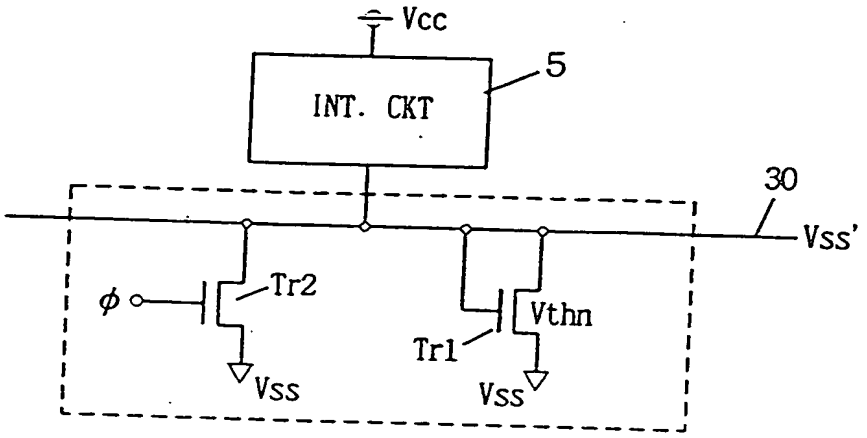

Vcc
INT. CKT
5
30
Vss'
φ
Tr2
Vss
Tr1
Vthn
Vss

FIG. 3

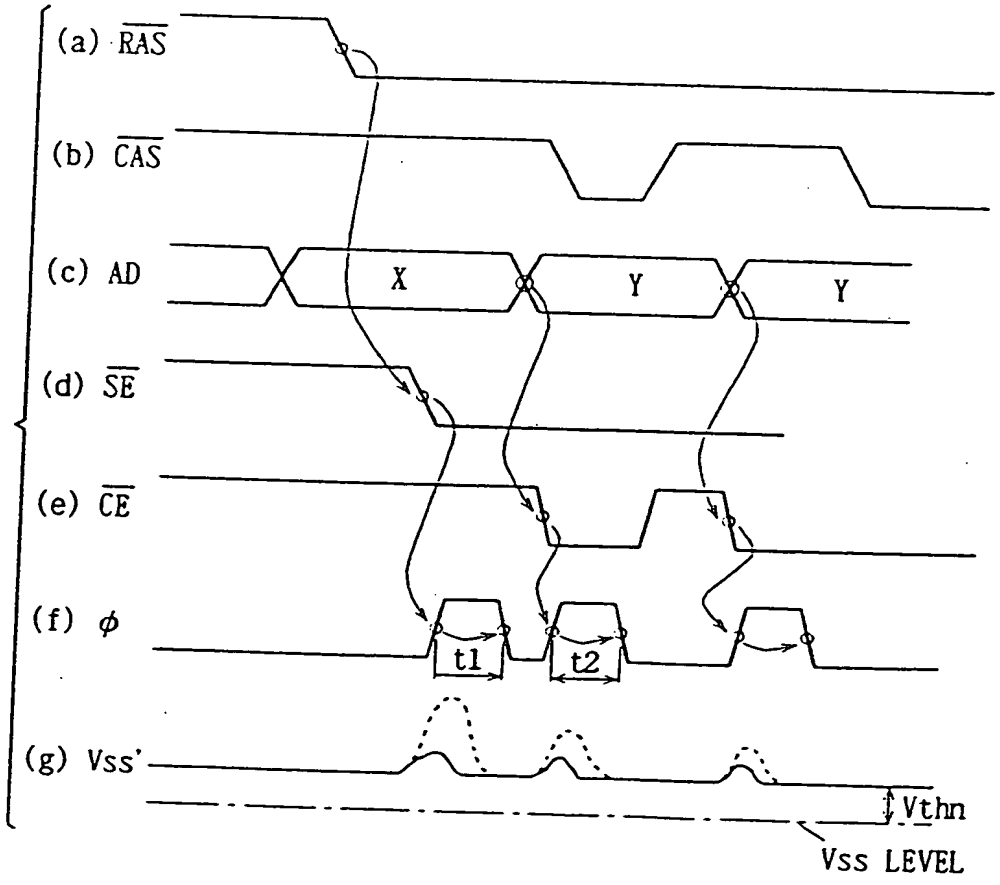

(a) $\overline{RAS}$
(b) $\overline{CAS}$
(c) AD
X
Y
Y
(d) $\overline{SE}$
(e) $\overline{CE}$
(f) φ
t1
t2
(g) Vss'
Vthn
Vss LEVEL

FIG. 4

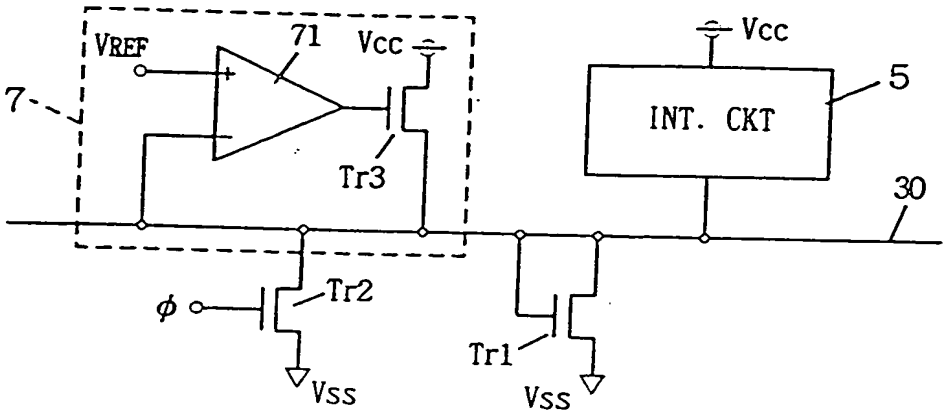

VREF
71
Vcc
7
Tr3
Vcc
INT. CKT
5
30
Tr2
ϕ
Vss
Tr1
Vss

FIG. 5

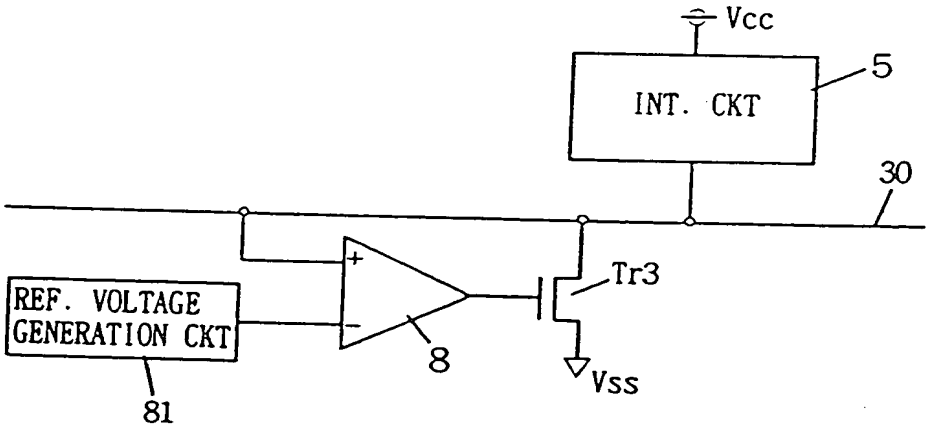

Vcc
INT. CKT
5
30
Tr3
REF. VOLTAGE GENERATION CKT
8
Vss
81

FIG. 6

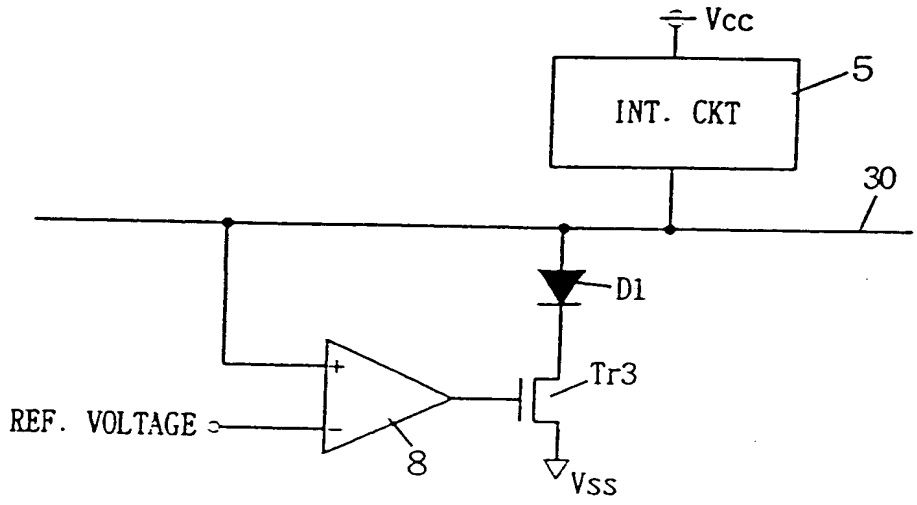

Vcc
INT. CKT
5
30
D1
Tr3
REF. VOLTAGE
8
Vss

FIG. 7

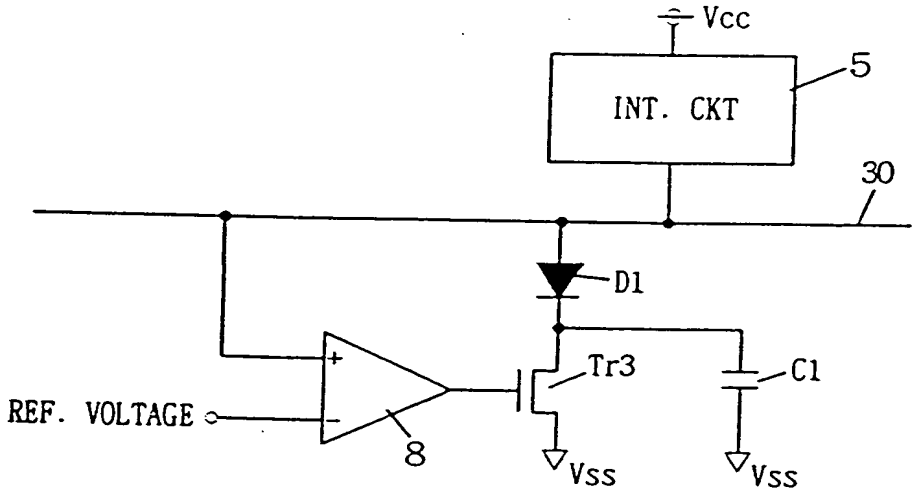

Vcc
INT. CKT
5
30
D1
Tr3
C1
REF. VOLTAGE
8
Vss
Vss

FIG. 8

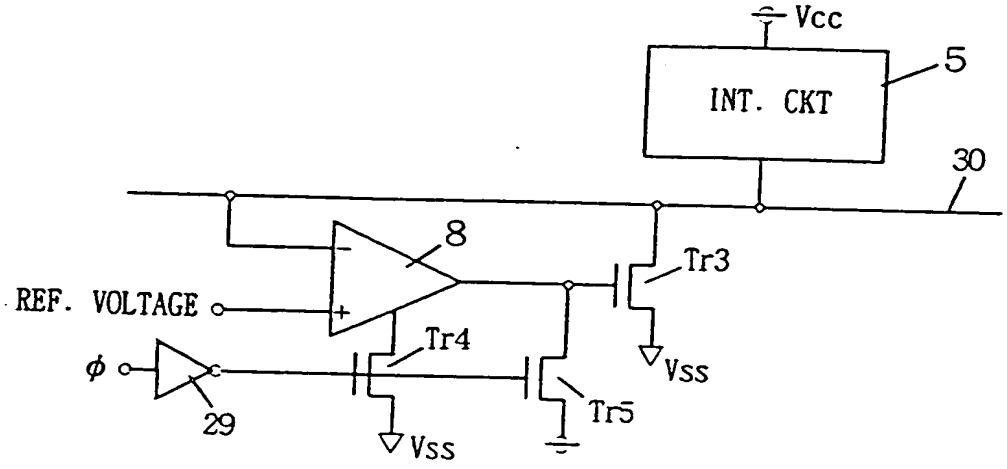

Vcc
INT. CKT
5
30
8
Tr3
REF. VOLTAGE
Tr4
Vss
φ
29
Tr5
Vss

FIG. 9

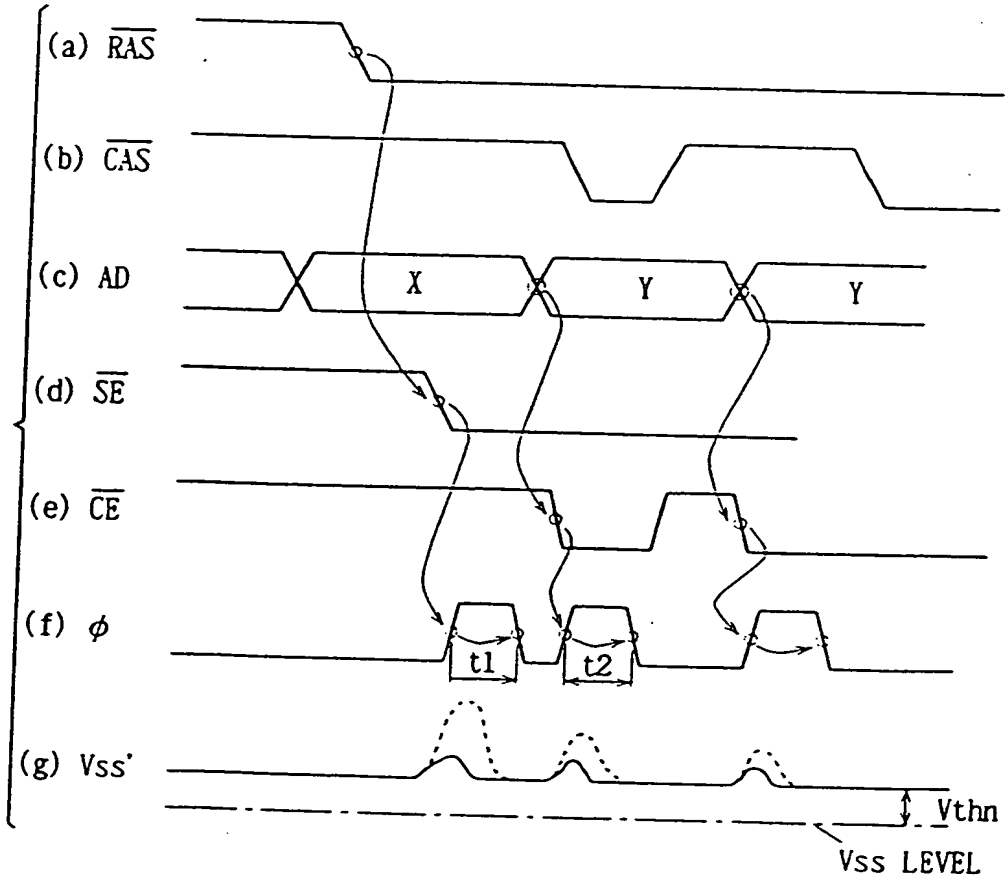

(a) $\overline{RAS}$
(b) $\overline{CAS}$
(c) AD
X
Y
Y
(d) $\overline{SE}$
(e) $\overline{CE}$
(f) φ
t1
t2
(g) Vss'
Vthn
Vss LEVEL

FIG. 10

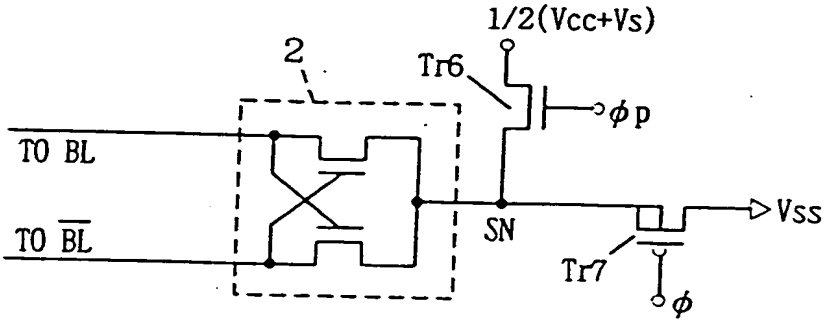

1/2(Vcc+Vs)
2
Tr6
φp
TO BL
TO $\overline{BL}$
SN
Vss
Tr7
φ

FIG. 11

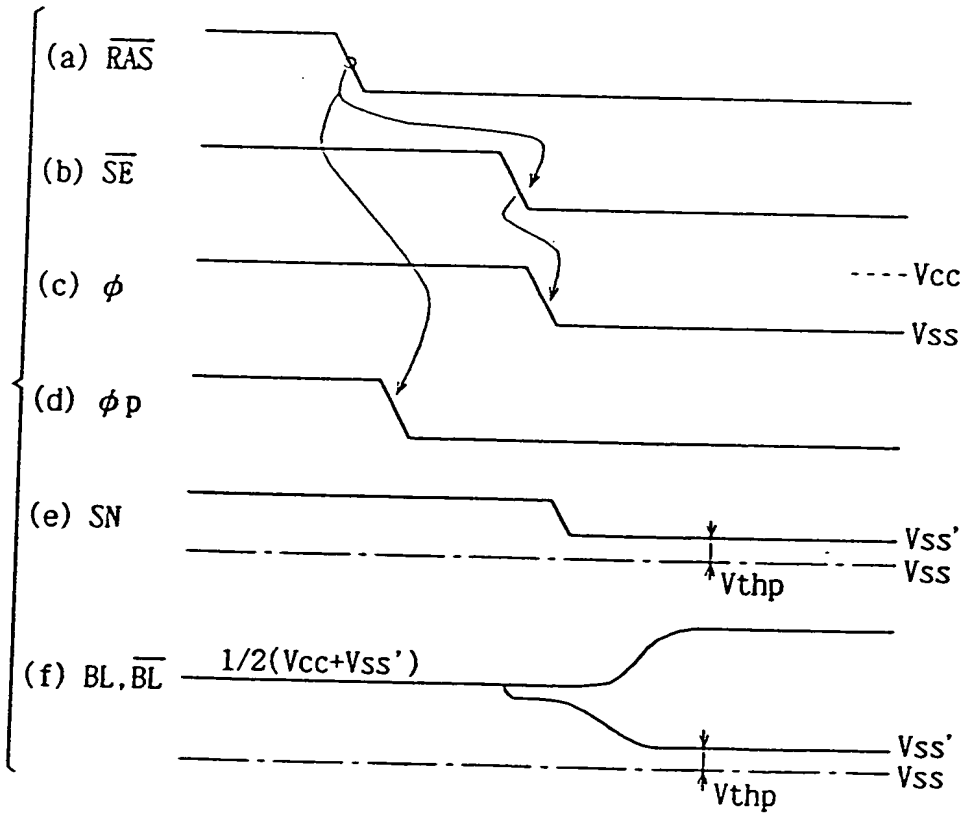

(a) $\overline{RAS}$
(b) $\overline{SE}$
(c) φ
(d) φp
(e) SN
(f) BL, $\overline{BL}$
Vcc
Vss
Vss'
Vss
Vthp
1/2(Vcc+Vss')
Vss'
Vss
Vthp

FIG. 12

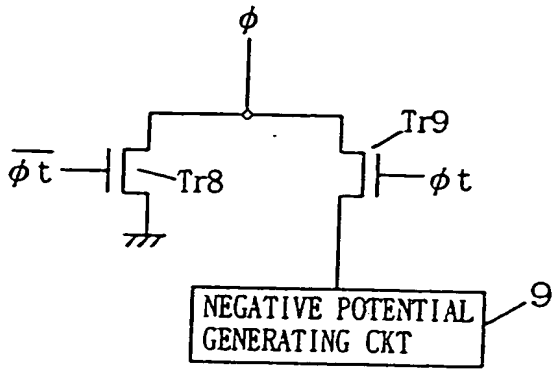

φ
Tr9
φt
Tr8
φt
NEGATIVE POTENTIAL GENERATING CKT
9

FIG. 13

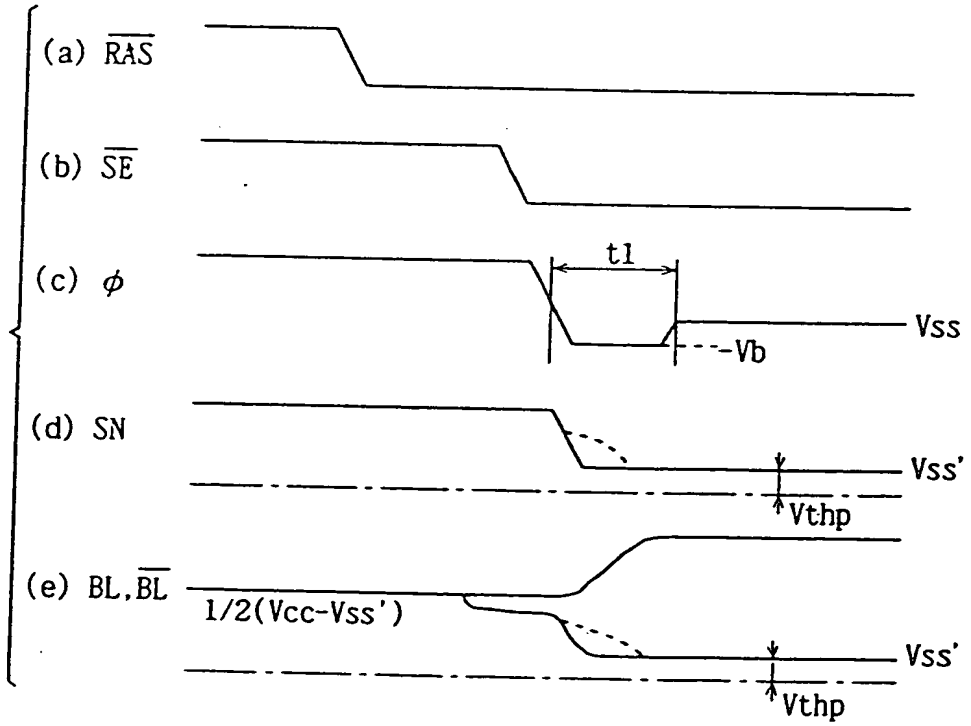

(a) RAS
(b) SE
(c) φ
t1
Vss
Vb
(d) SN
Vss'
Vthp
(e) BL, BL
1/2(Vcc-Vss')
Vss'
Vthp

FIG. 14

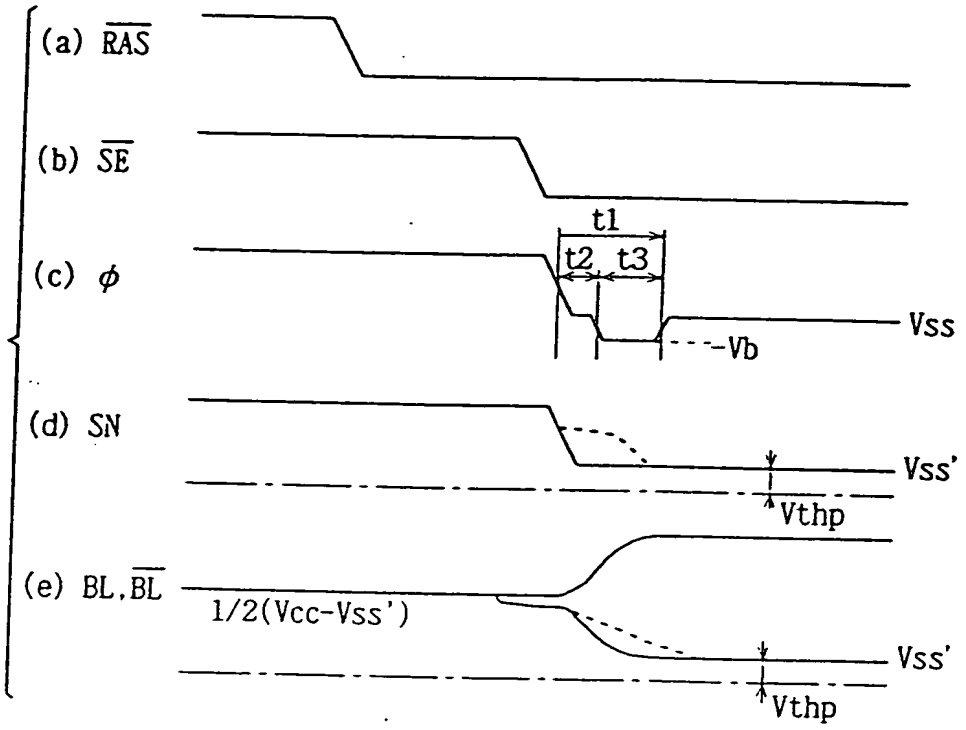

(a) $\overline{RAS}$
(b) $\overline{SE}$
(c) ϕ
t1
t2
t3
Vss
Vb
(d) SN
Vss'
Vthp
(e) BL, $\overline{BL}$
1/2(Vcc-Vss')
Vss'
Vthp

FIG. 15

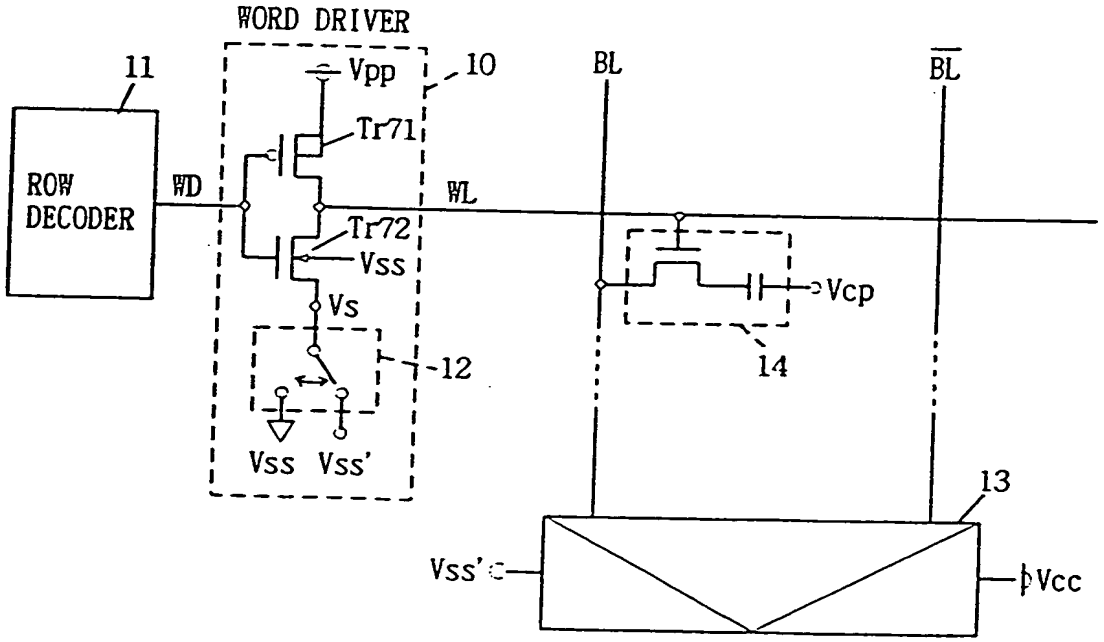

WORD DRIVER
11
10
Vpp
Tr71
ROW DECODER
WD
WL
Tr72
Vss
Vs
12
Vss Vss'
BL
$\overline{BL}$
Vcp
14
13
Vss'
Vcc

FIG. 16

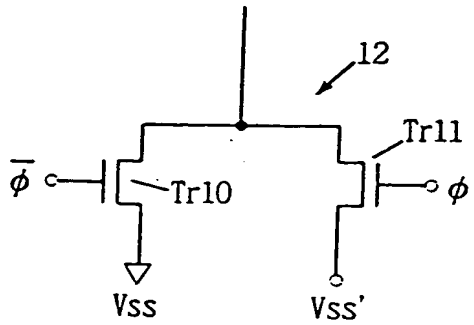

12
Tr11
$\overline{\phi}$
Tr10
ϕ
Vss
Vss'

FIG. 17

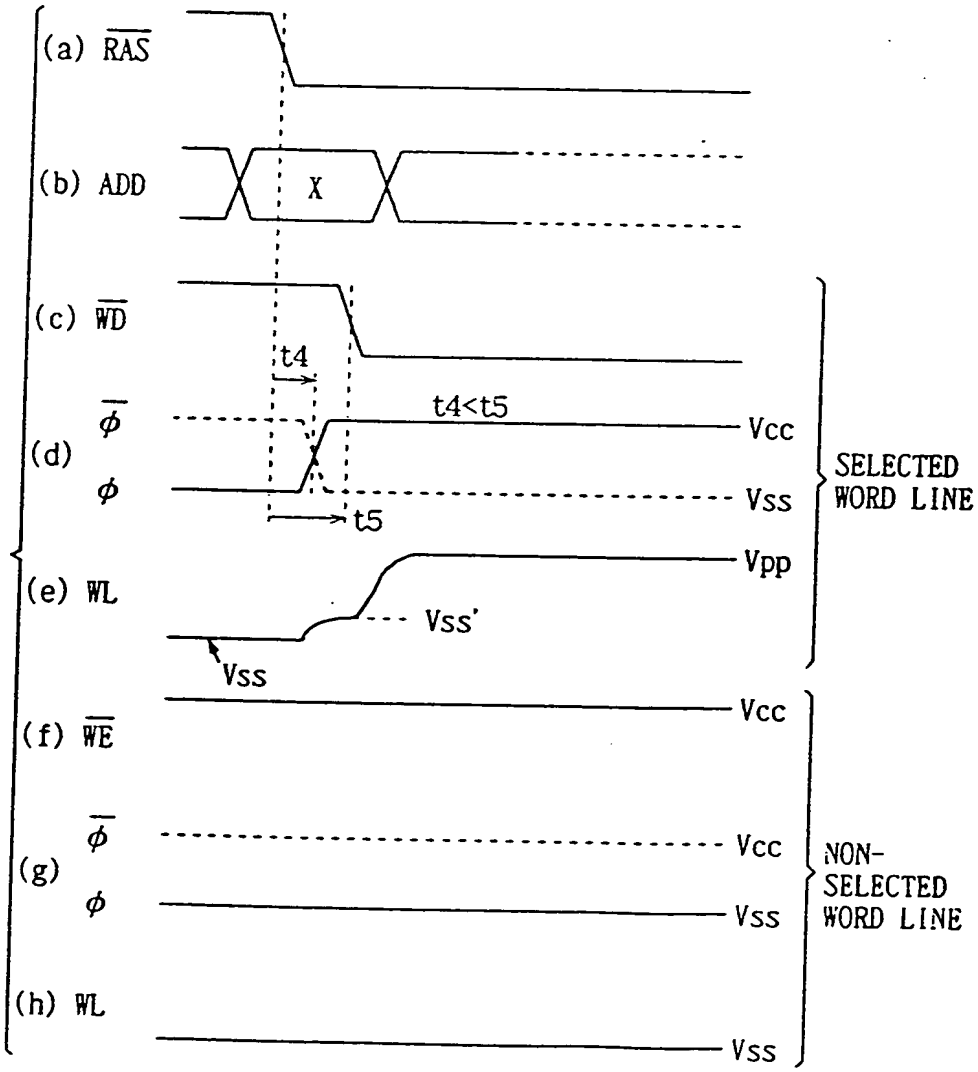

(a) $\overline{RAS}$
(b) ADD
X
(c) $\overline{WD}$
t4
t4<t5
(d) $\overline{\phi}$
ϕ
Vcc
Vss
t5
SELECTED WORD LINE
(e) WL
Vpp
Vss'
Vss
(f) $\overline{WE}$
Vcc
(g) $\overline{\phi}$
ϕ
Vcc
Vss
NON-SELECTED WORD LINE
(h) WL
Vss

FIG. 18

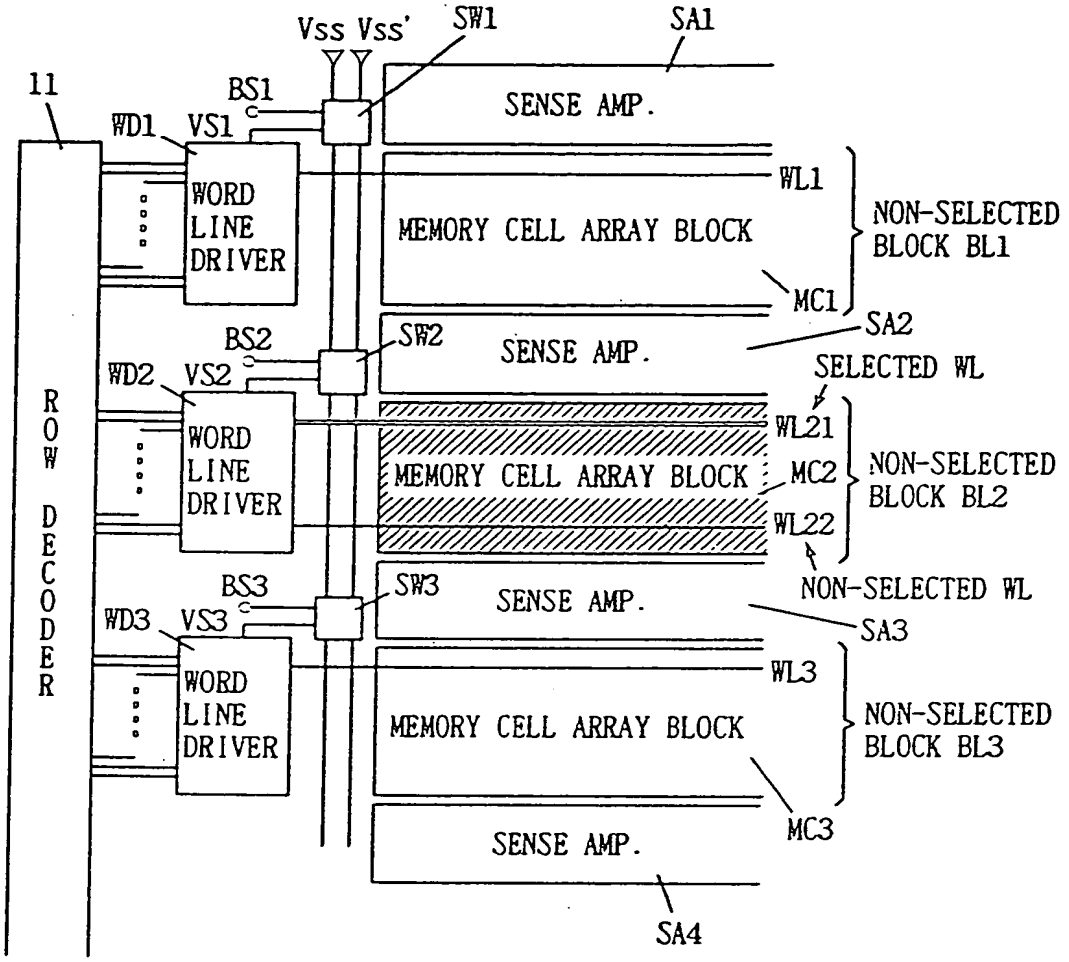

Vss Vss'
SW1
SA1
11
BS1
WD1
VS1
SENSE AMP.
WORD LINE DRIVER
WL1
MEMORY CELL ARRAY BLOCK
NON-SELECTED BLOCK BL1
MC1
SA2
BS2
SW2
SENSE AMP.
SELECTED WL
WD2
VS2
WL21
WORD LINE DRIVER
MEMORY CELL ARRAY BLOCK
MC2
NON-SELECTED BLOCK BL2
WL22
NON-SELECTED WL
ROW DECODER
BS3
SW3
SENSE AMP.
SA3
WD3
VS3
WL3
WORD LINE DRIVER
MEMORY CELL ARRAY BLOCK
NON-SELECTED BLOCK BL3
MC3
SENSE AMP.
SA4

FIG. 19

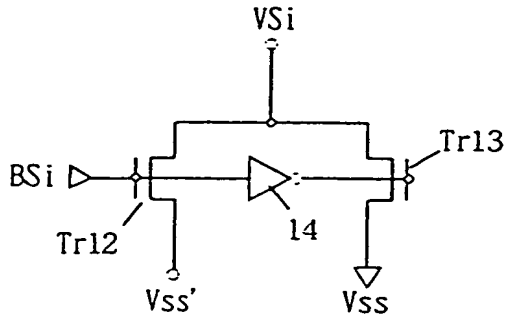

VSi
Tr13
BSi
Tr12
14
Vss'
Vss

FIG. 20

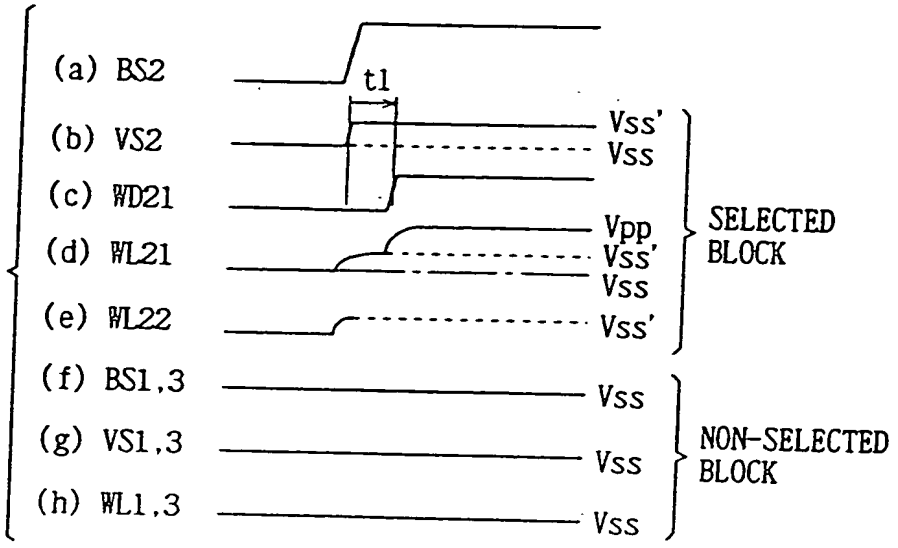

(a) BS2
t1
(b) VS2
Vss'
Vss
(c) WD21
Vpp
(d) WL21
Vss'
Vss
SELECTED BLOCK
(e) WL22
Vss'
(f) BS1,3
Vss
(g) VS1,3
Vss
NON-SELECTED BLOCK
(h) WL1,3
Vss

FIG. 21

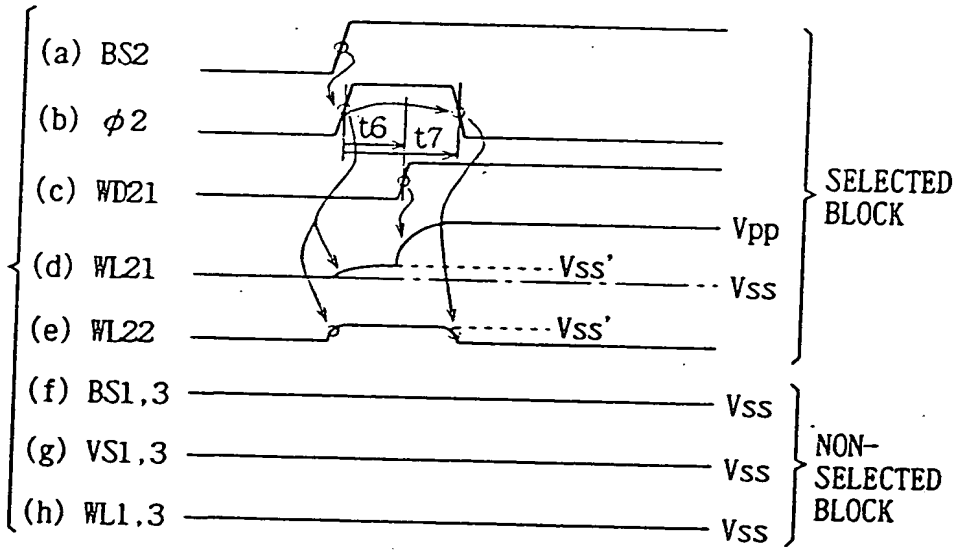

(a) BS2
(b) φ2
t6
t7
(c) WD21
Vpp
(d) WL21
Vss'
Vss
SELECTED BLOCK
(e) WL22
Vss'
(f) BS1,3
Vss
(g) VS1,3
Vss
NON-SELECTED BLOCK
(h) WL1,3
Vss

FIG. 22

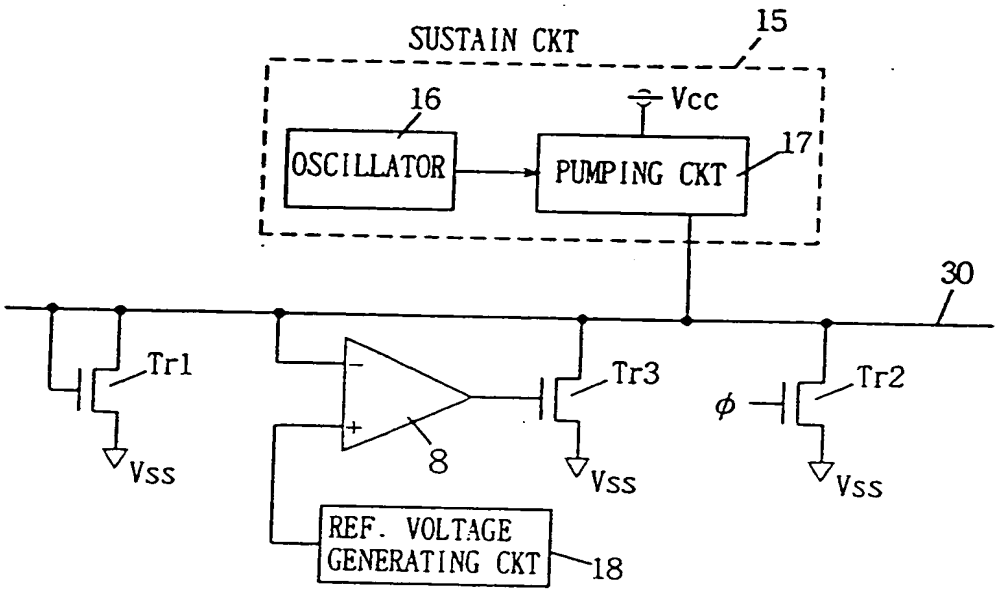

SUSTAIN CKT
15
16
Vcc
OSCILLATOR
PUMPING CKT
17
30
Tr1
Tr3
Tr2
φ
Vss
Vss
Vss
8
REF. VOLTAGE
GENERATING CKT
18

FIG. 23

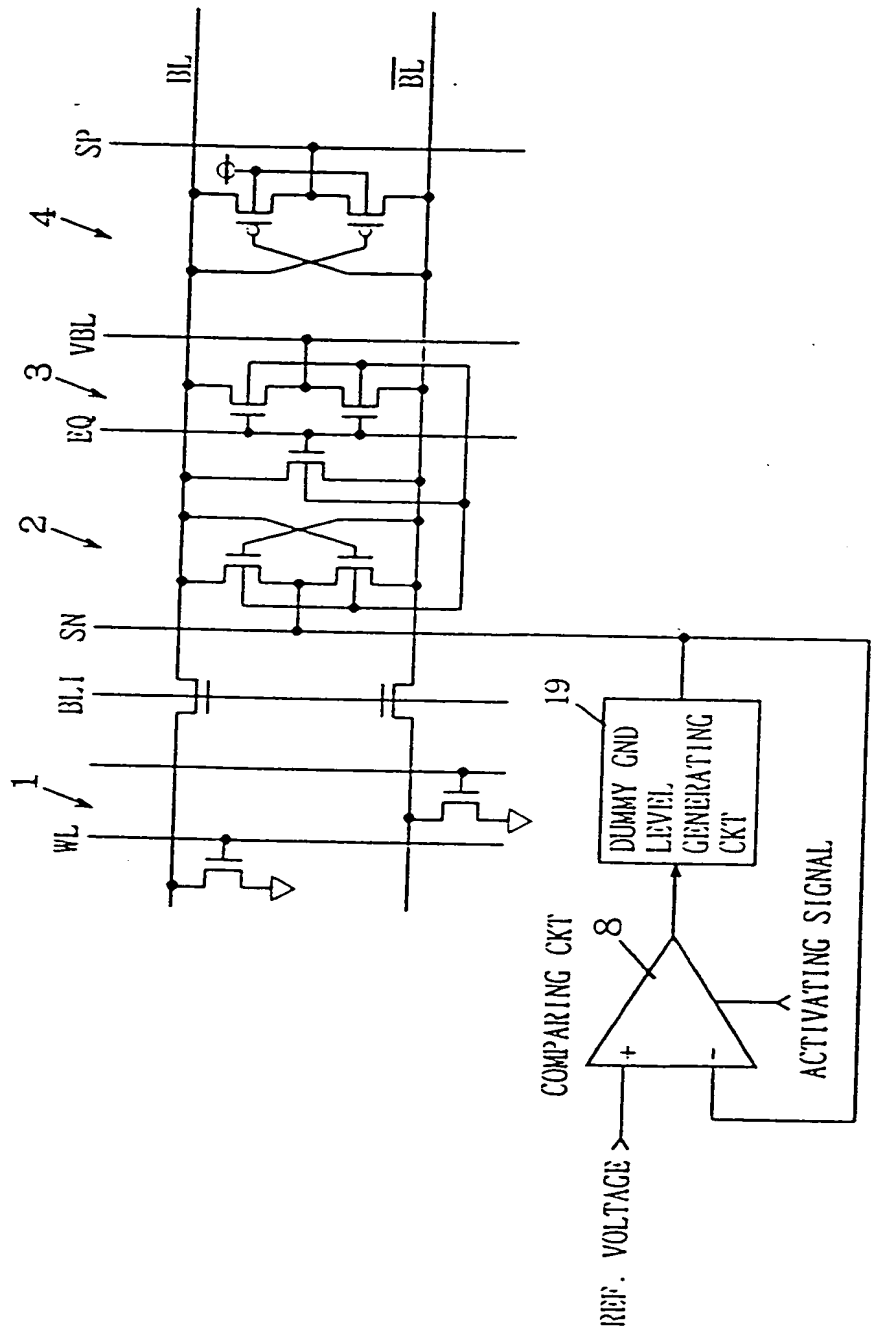

WL
BLI
SN
EQ
VBL
SP
BL
$\overline{BL}$
1
2
3
4
19
DUMMY GND LEVEL GENERATING CKT
8
COMPARING CKT
+
-
REF. VOLTAGE
ACTIVATING SIGNAL

FIG. 24

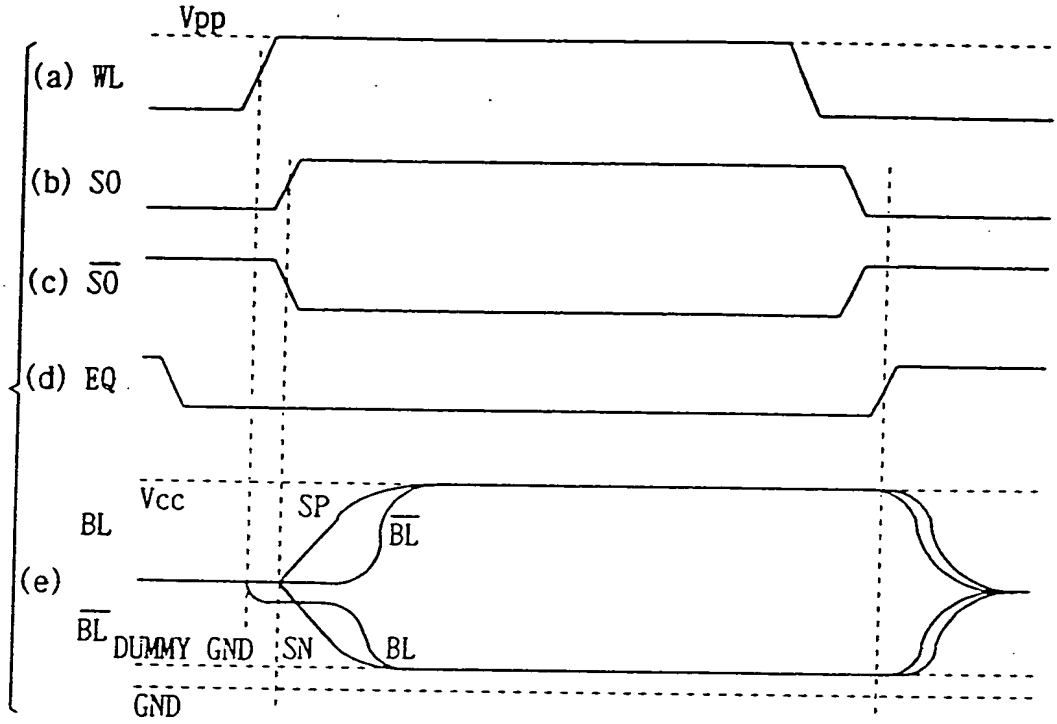

Vpp
(a) WL
(b) SO
(c) $\overline{SO}$
(d) EQ
Vcc
SP
BL
$\overline{BL}$
(e)
$\overline{BL}$
DUMMY GND
SN
BL
GND

FIG. 25

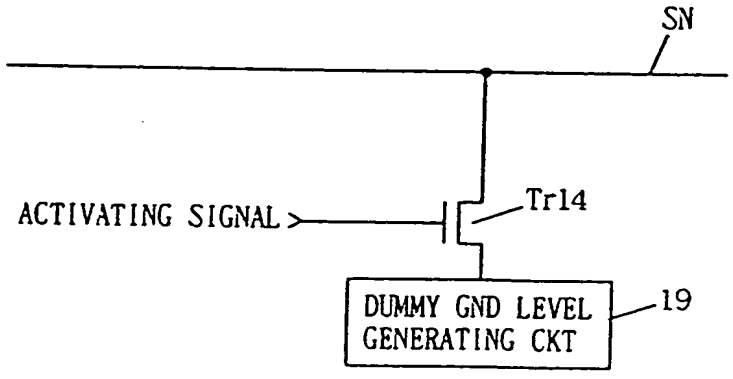

SN
ACTIVATING SIGNAL
Tr14
DUMMY GND LEVEL GENERATING CKT
19

FIG. 26

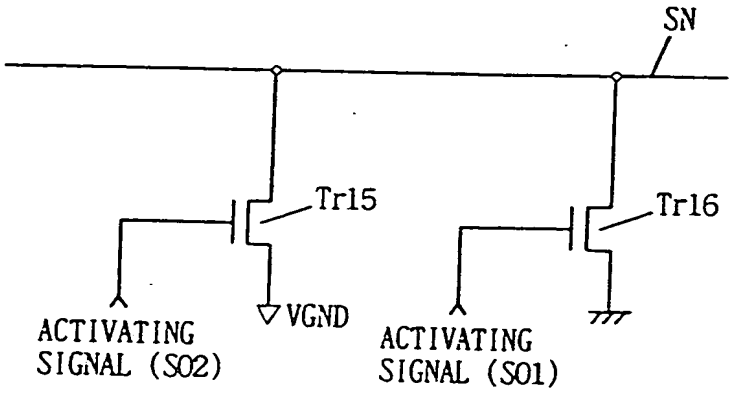

SN
Tr15
Tr16
VGND
ACTIVATING SIGNAL (SO2)
ACTIVATING SIGNAL (SO1)

FIG. 27

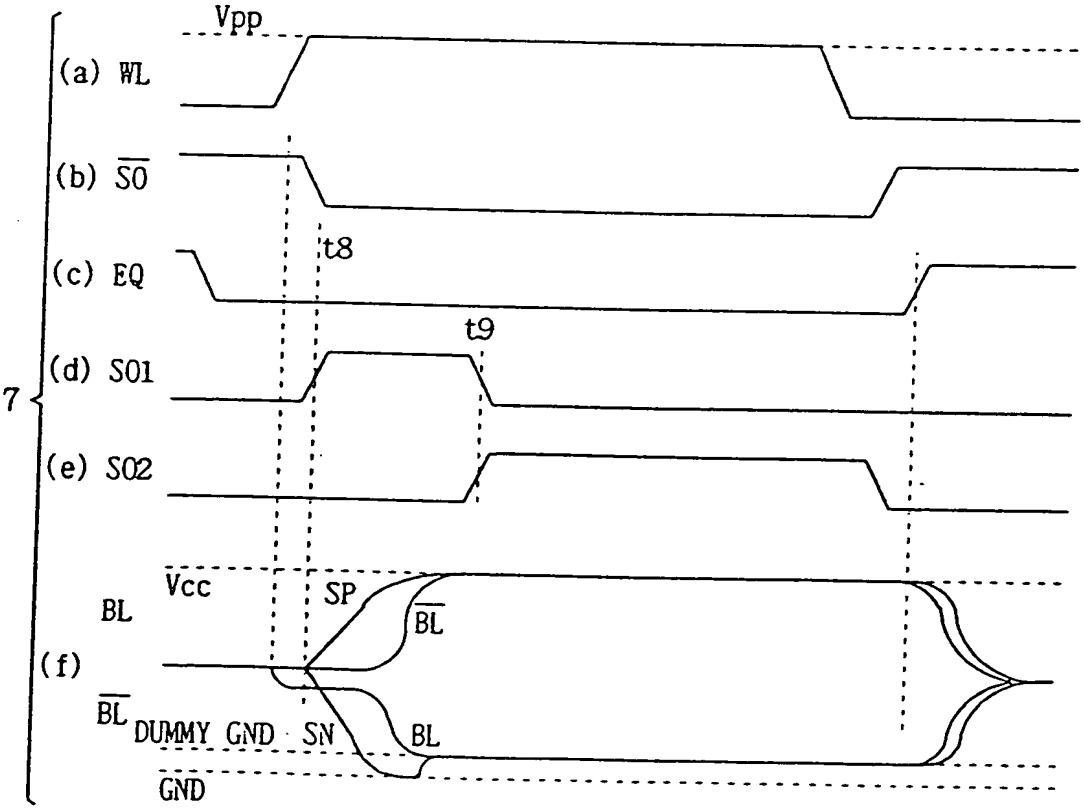

Vpp
(a) WL
(b) $\overline{SO}$
t8
(c) EQ
t9
(d) SO1
(e) SO2
Vcc
SP
BL
$\overline{BL}$
(f)
$\overline{BL}$
DUMMY GND
SN
BL
GND

FIG. 28

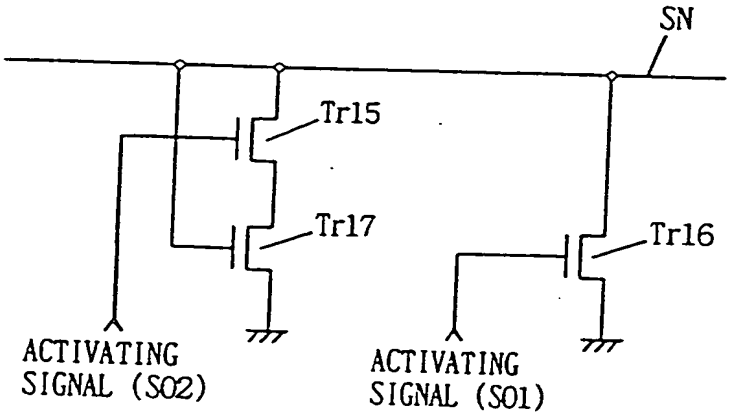

SN
Tr15
Tr17
Tr16
ACTIVATING SIGNAL (SO2)
ACTIVATING SIGNAL (SO1)

FIG. 29

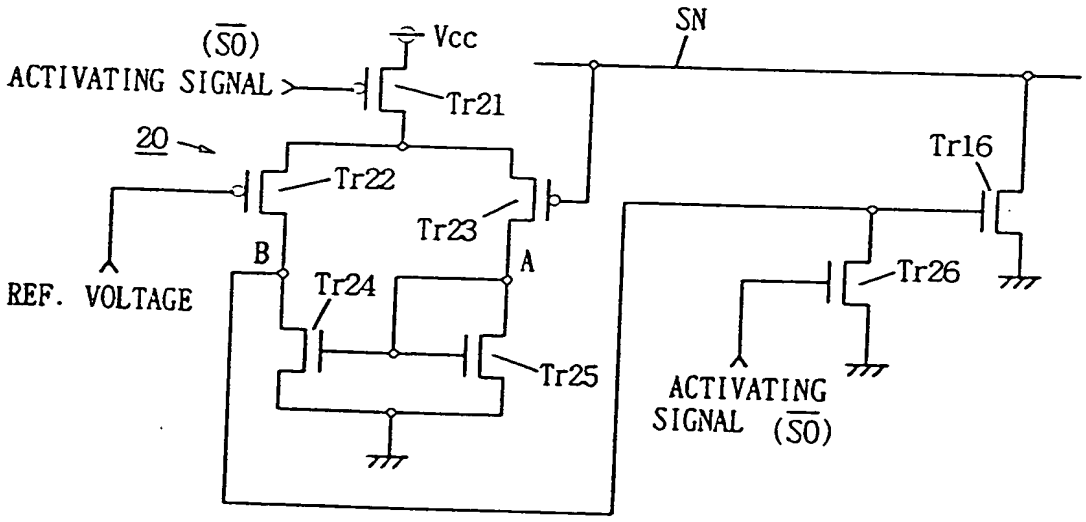

(S0)
ACTIVATING SIGNAL
Vcc
SN
Tr21
20
Tr22
Tr23
Tr16
B
A
REF. VOLTAGE
Tr24
Tr26
Tr25
ACTIVATING SIGNAL (S0)

FIG. 30

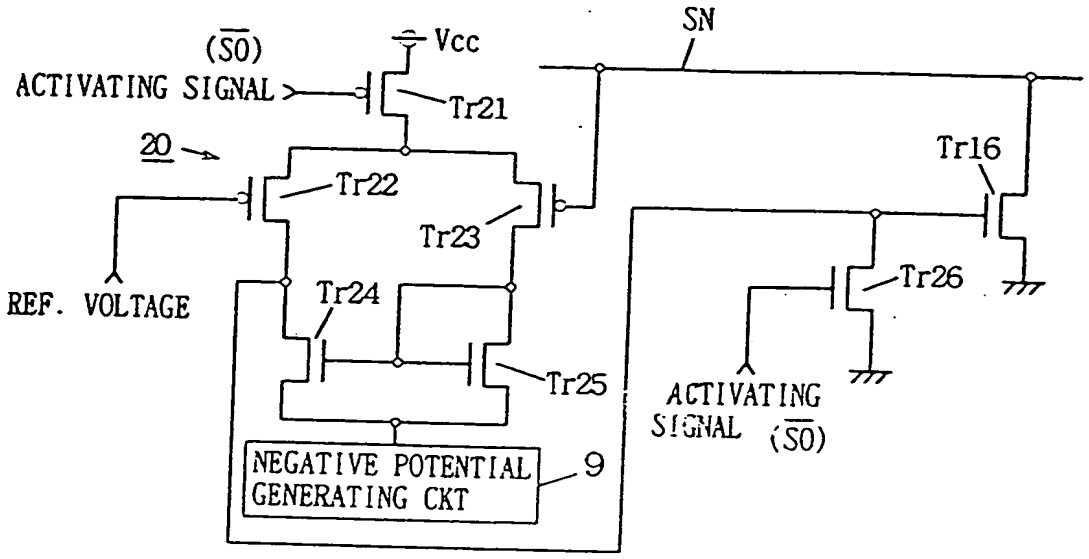

(S0)
ACTIVATING SIGNAL
Vcc
Tr21
SN
20
Tr22
Tr23
Tr16
Tr26
REF. VOLTAGE
Tr24
Tr25
ACTIVATING SIGNAL (S0)
NEGATIVE POTENTIAL GENERATING CKT
9

FIG. 31

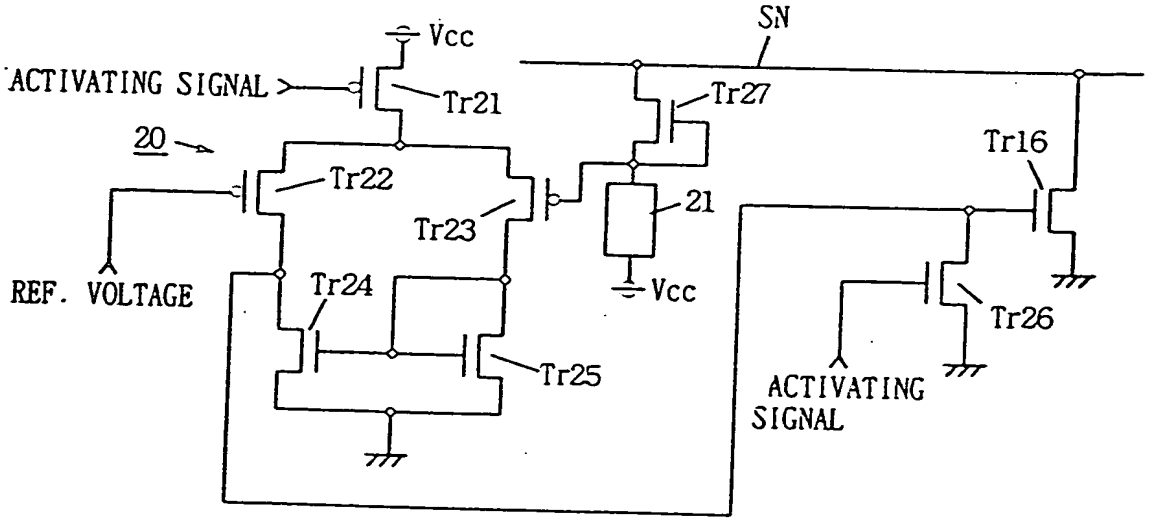

Vcc
SN
ACTIVATING SIGNAL
Tr21
Tr27
20
Tr22
Tr16
21
Tr23
REF. VOLTAGE
Tr24
Vcc
Tr26
Tr25
ACTIVATING SIGNAL

FIG. 32

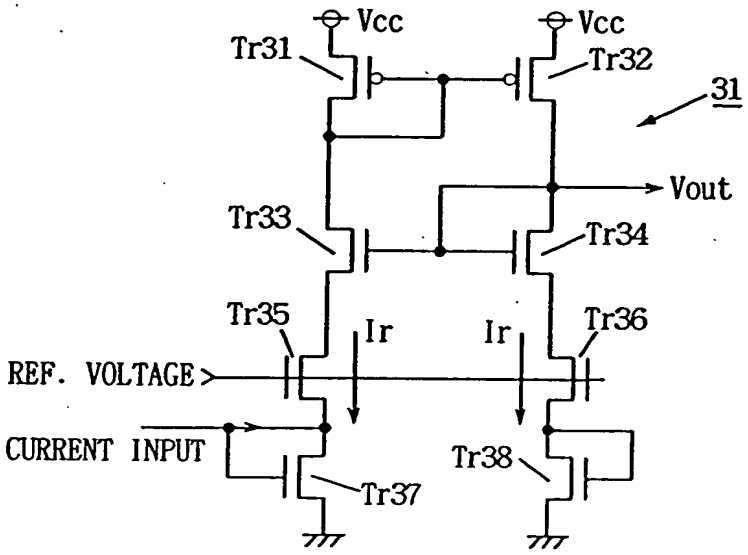

Vcc
Vcc
Tr31
Tr32
31
Vout
Tr33
Tr34
Tr35
Ir
Ir
Tr36
REF. VOLTAGE
CURRENT INPUT
Tr38
Tr37

FIG. 33

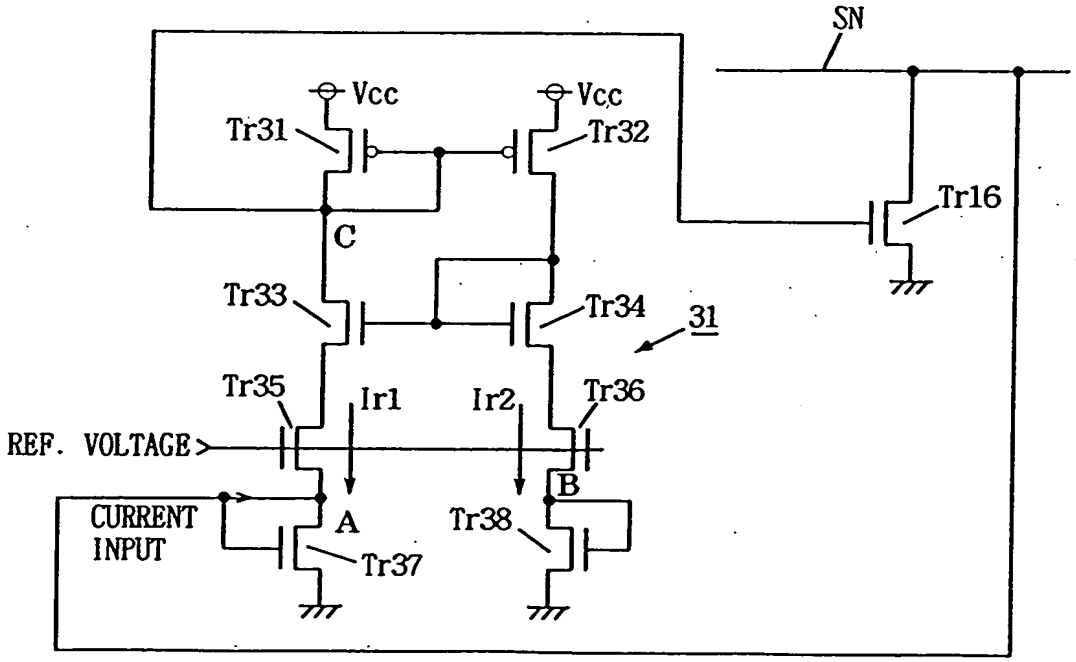

SN
Vcc
Vcc
Tr31
Tr32
Tr16
C
Tr33
Tr34
31
Tr35
Ir1
Ir2
Tr36
REF. VOLTAGE
B
CURRENT INPUT
A
Tr38
Tr37

FIG. 34

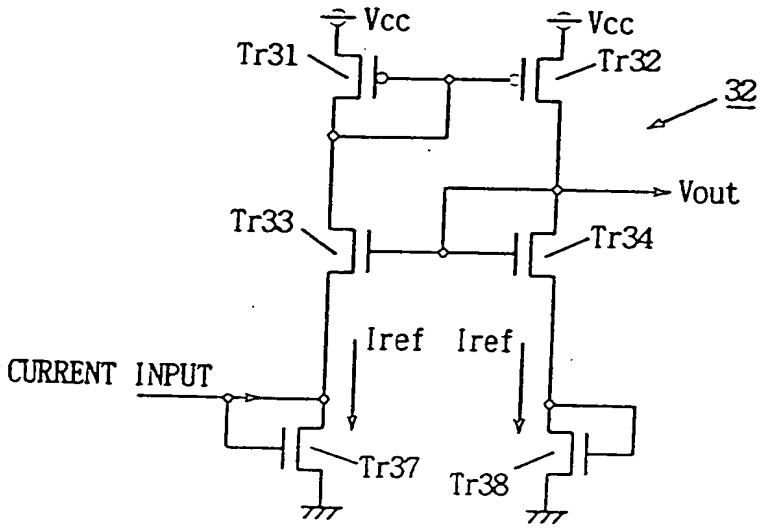

Vcc
Vcc
Tr31
Tr32
32
Vout
Tr33
Tr34
Iref
Iref
CURRENT INPUT
Tr37
Tr38

FIG. 35

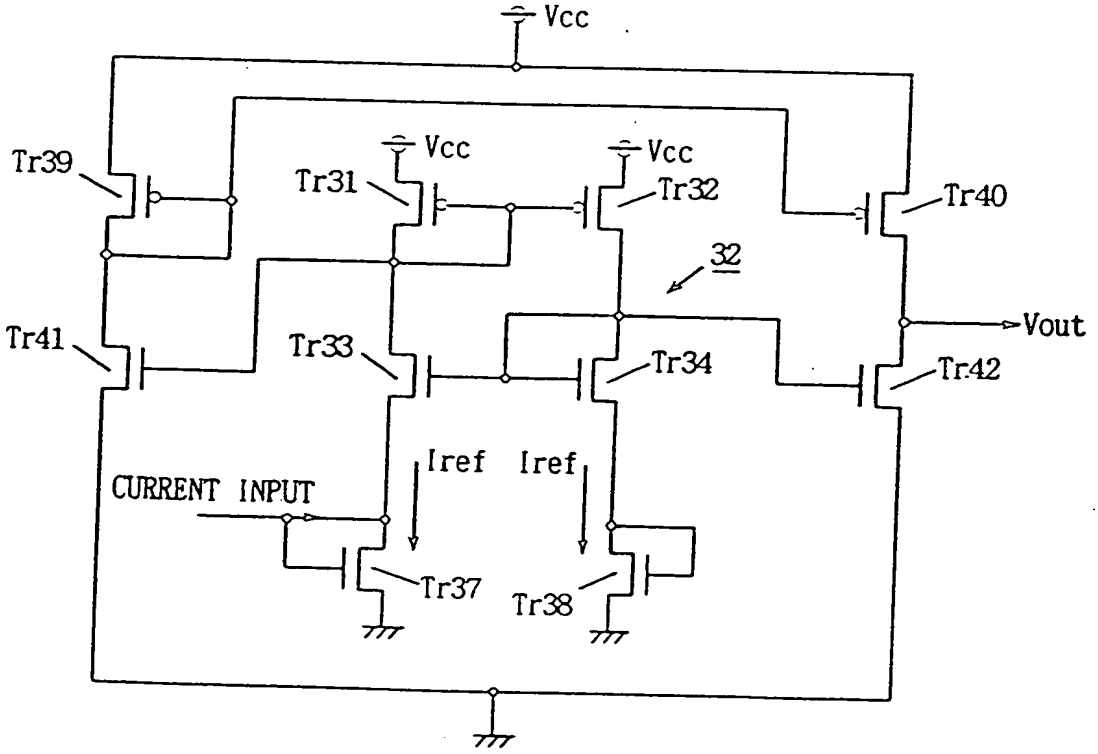

Vcc
Tr39
Vcc
Vcc
Tr31
Tr32
Tr40
32
Tr41
Tr33
Tr34
Tr42
Vout
Iref
Iref
CURRENT INPUT
Tr37
Tr38

FIG. 36

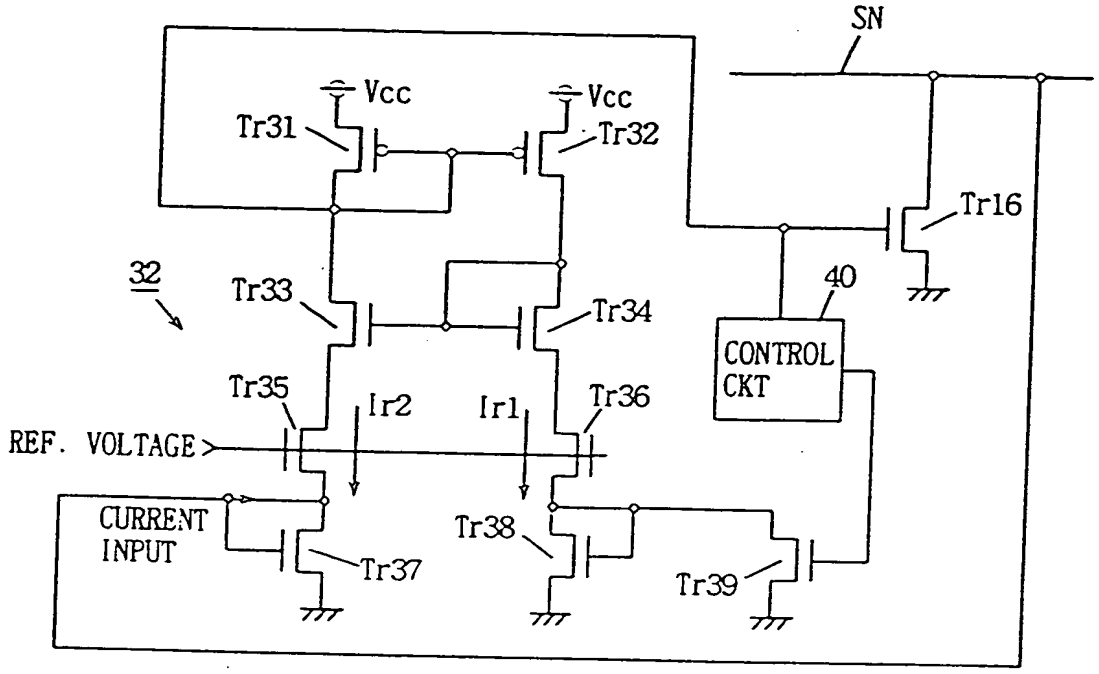

SN
Vcc
Vcc
Tr31
Tr32
Tr16
32
Tr33
Tr34
40
CONTROL CKT
Tr35
Ir2
Ir1
Tr36
REF. VOLTAGE
CURRENT INPUT
Tr37
Tr38
Tr39

FIG. 37

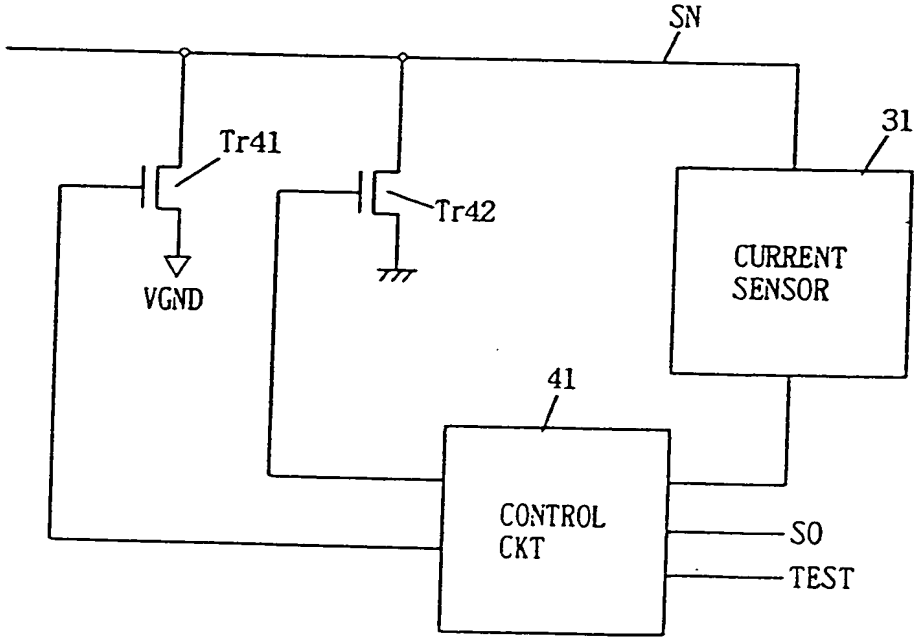

SN
Tr41
Tr42
31
VGND
CURRENT SENSOR
41
CONTROL CKT
SO
TEST

FIG. 38

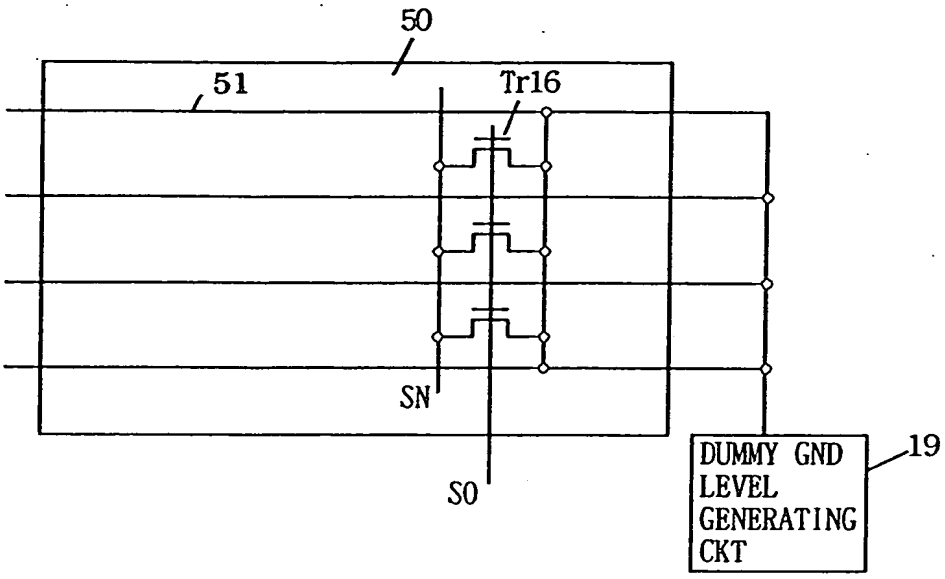

50
51
Tr16
SN
SO
DUMMY GND LEVEL GENERATING CKT
19

FIG. 39

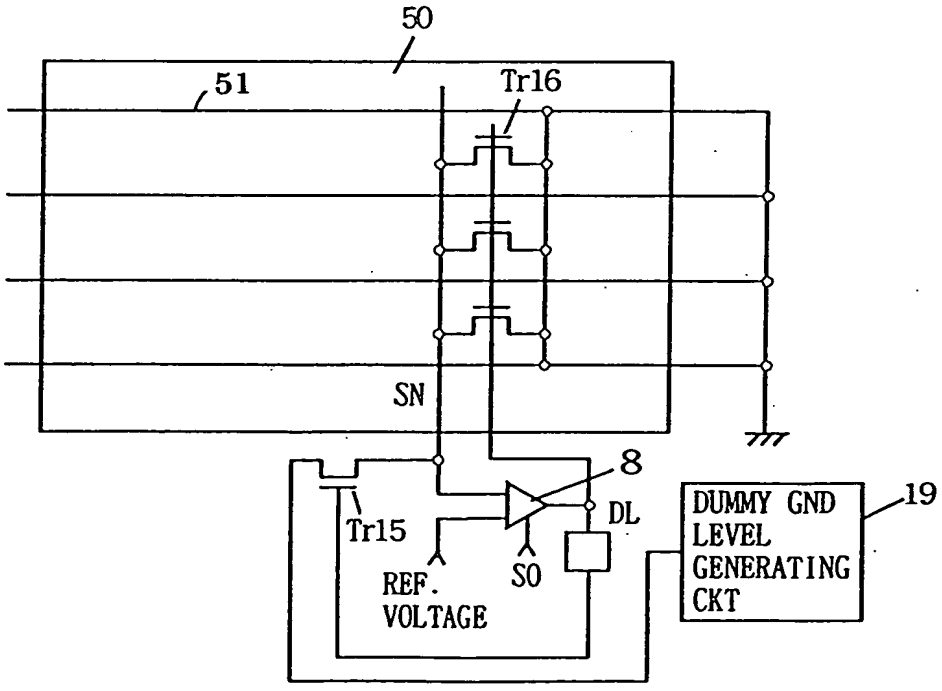

50
51
Tr16
SN
8
DL
Tr15
REF. VOLTAGE
SO
DUMMY GND LEVEL GENERATING CKT
19

FIG. 40

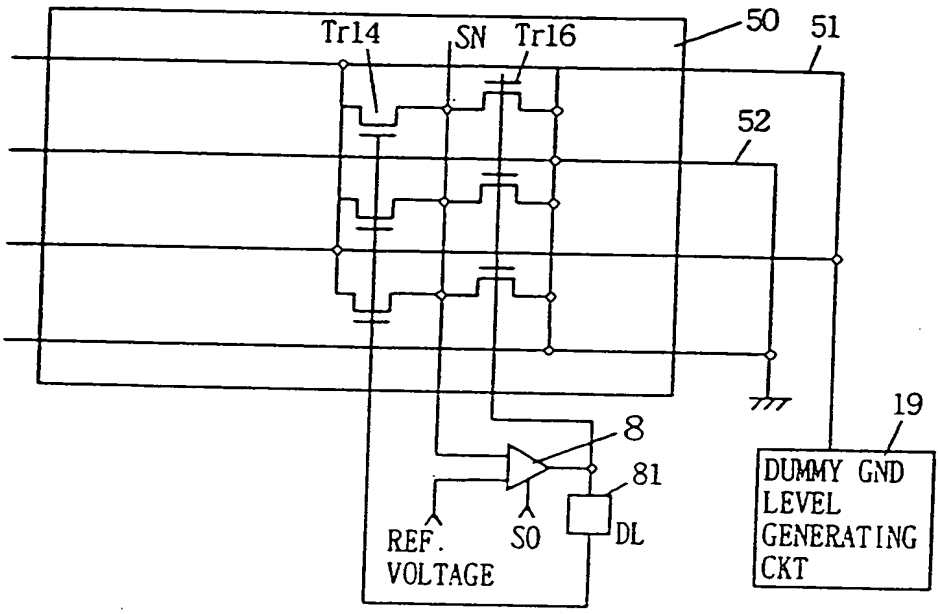

Tr14
SN
Tr16
50
51
52
19
8
81
DL
SO
REF.
VOLTAGE
DUMMY GND
LEVEL
GENERATING
CKT

FIG. 41

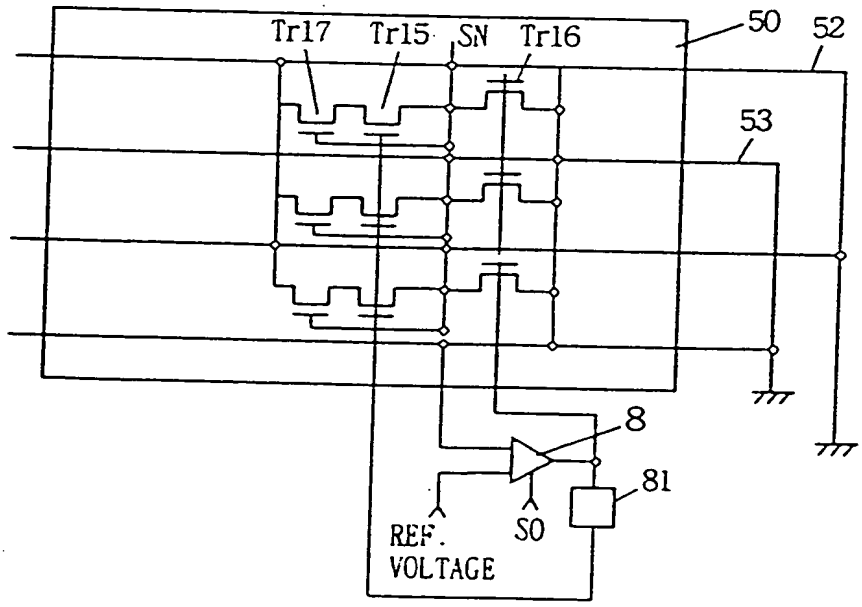

Tr17
Tr15
SN
Tr16
50
52
53
8
81
SO
REF.
VOLTAGE

FIG. 42

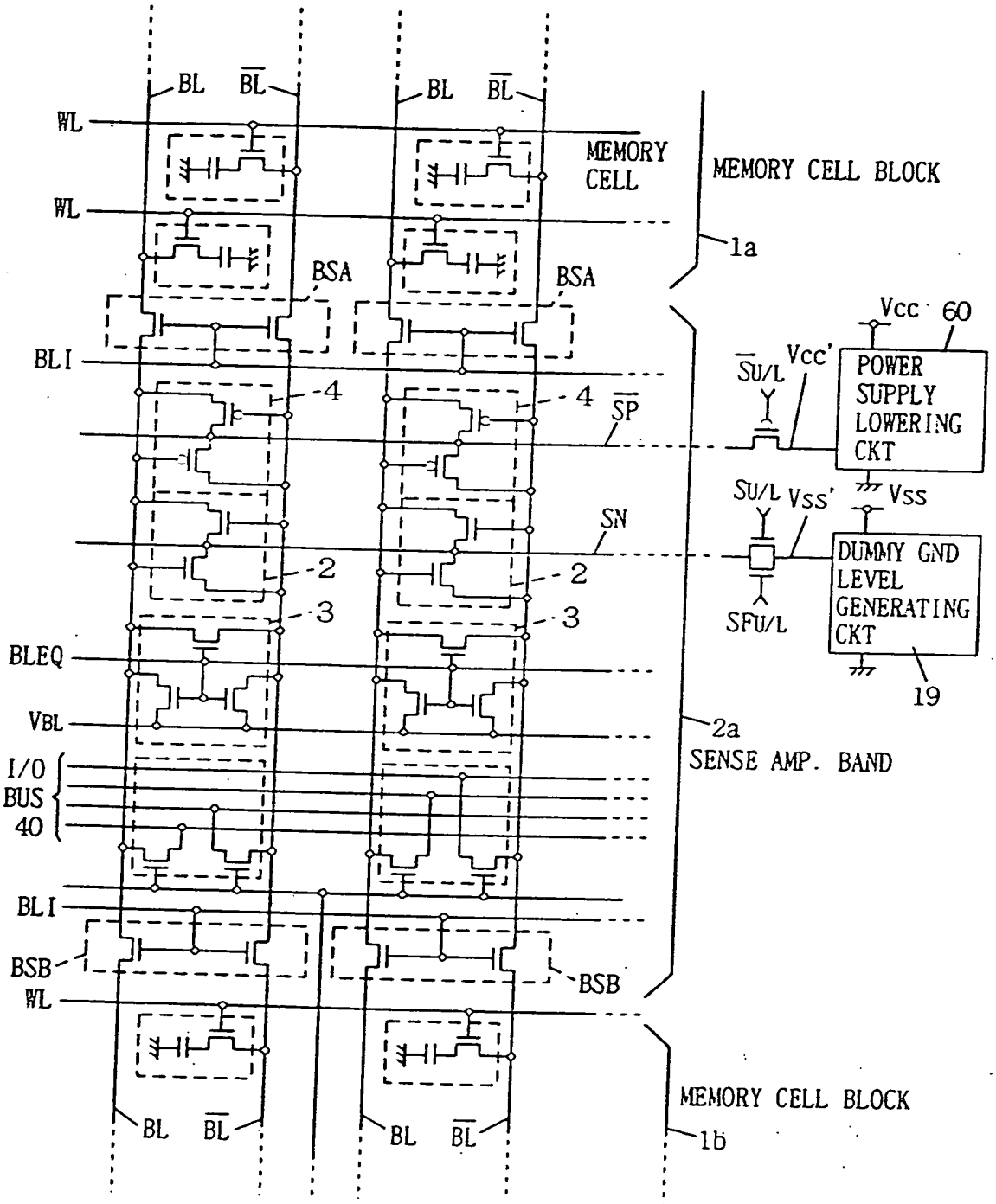

BL
BL
WL
MEMORY CELL
MEMORY CELL BLOCK
1a
BSA
Vcc
60
BLI
SU/L
Vcc'
POWER SUPPLY LOWERING CKT
4
SP
SU/L
Vss'
Vss
SN
DUMMY GND LEVEL GENERATING CKT
2
3
SFU/L
19
BLEQ
VBL
2a
SENSE AMP. BAND
I/O BUS 40
BSB
1b

FIG. 43

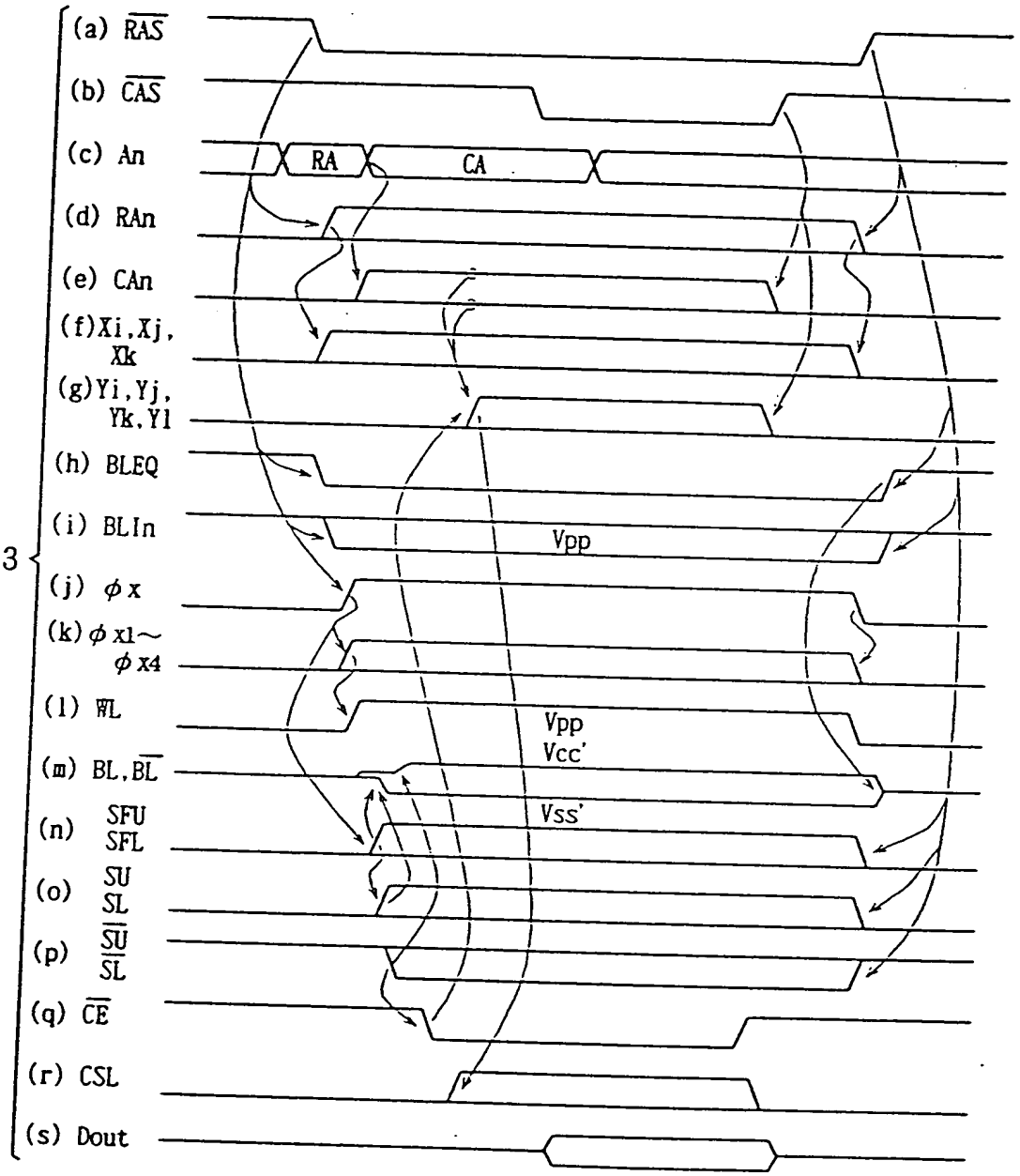

(a) $\overline{RAS}$
(b) $\overline{CAS}$
(c) An
RA
CA
(d) RAn
(e) CAn
(f) Xi, Xj, Xk
(g) Yi, Yj, Yk, Yl
(h) BLEQ
(i) BLIn
Vpp
(j) ϕx
(k) $\phi x1 \sim \phi x4$
(l) WL
Vpp
Vcc'
(m) BL, $\overline{BL}$
Vss'
(n) SFU SFL
(o) SU SL
(p) $\overline{SU}$ $\overline{SL}$
(q) $\overline{CE}$
(r) CSL
(s) Dout

FIG. 44

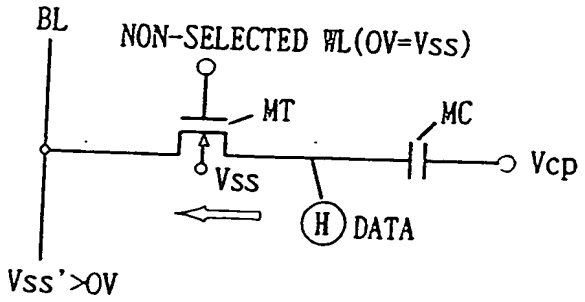

BL
NON-SELECTED WL(OV=Vss)
MT
MC
Vcp
Vss
H
DATA
Vss'>OV

FIG. 45

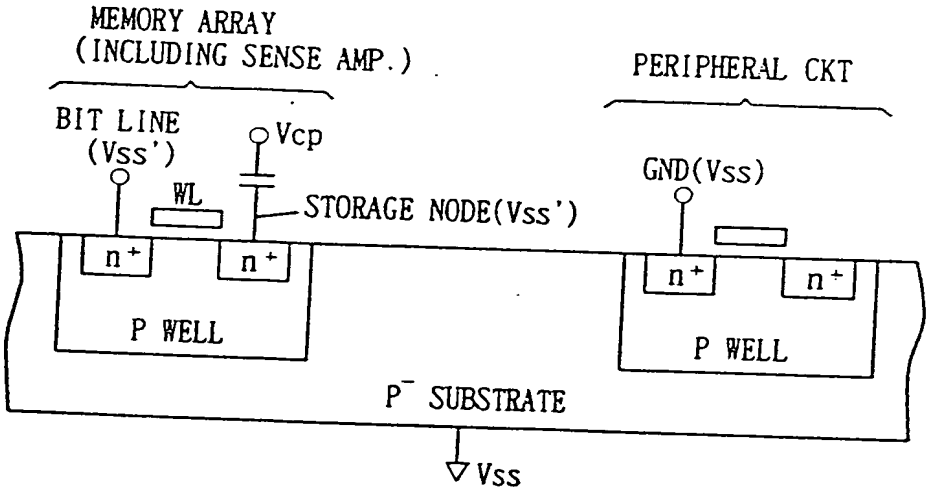

MEMORY ARRAY
(INCLUDING SENSE AMP.)
PERIPHERAL CKT
BIT LINE
(Vss')
Vcp
WL
STORAGE NODE(Vss')
GND(Vss)
n+
n+
n+
n+
P WELL
P WELL
P⁻ SUBSTRATE
Vss

FIG. 46

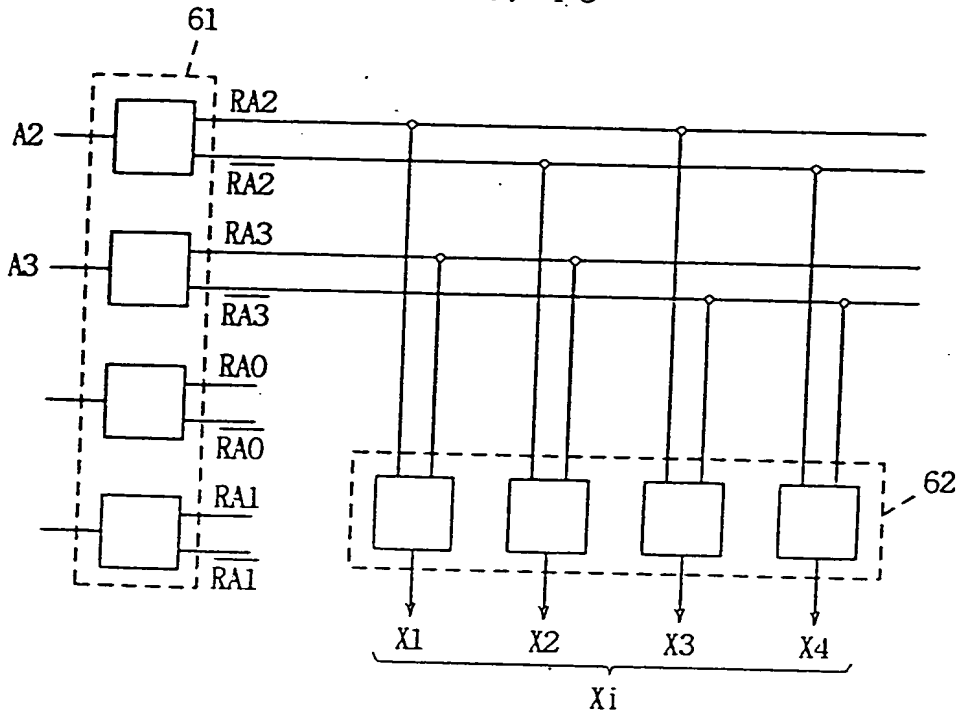

61
A2
A3
RA2
$\overline{RA2}$
RA3
$\overline{RA3}$
RA0
$\overline{RA0}$
RA1
$\overline{RA1}$
62
X1
X2
X3
X4
Xi

FIG. 47

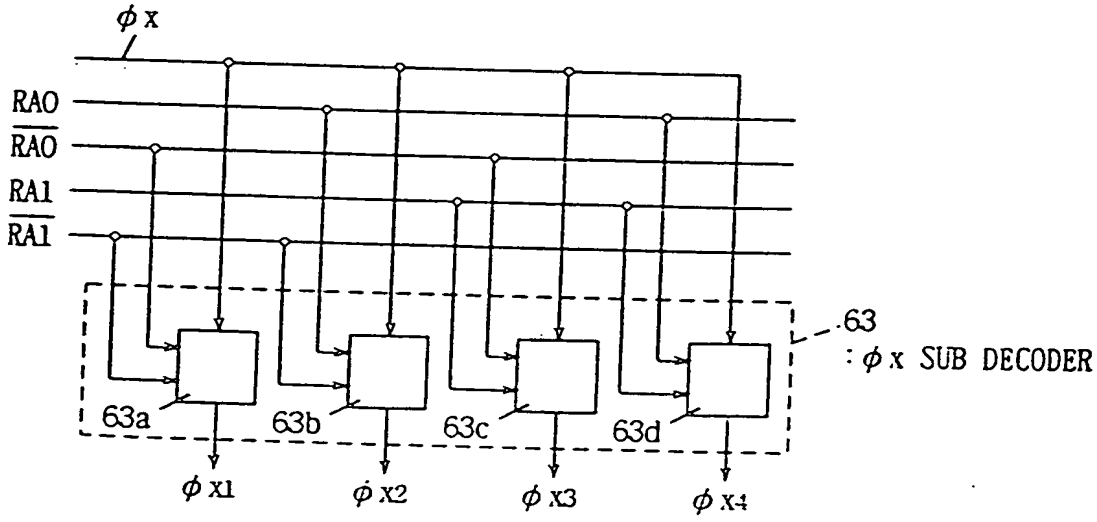

ϕx
RA0
$\overline{RA0}$
RA1
$\overline{RA1}$
63
: ϕx SUB DECODER
63a
63b
63c
63d
ϕx1
ϕx2
ϕx3
ϕx4

FIG. 48

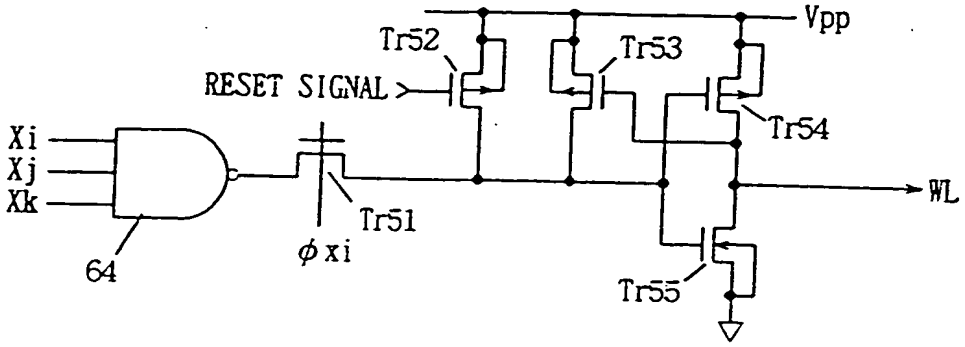


FIG. 49

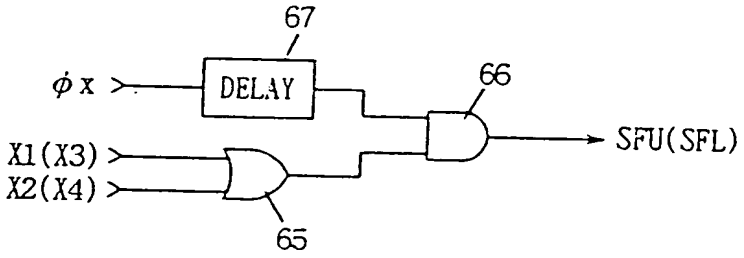


FIG. 50

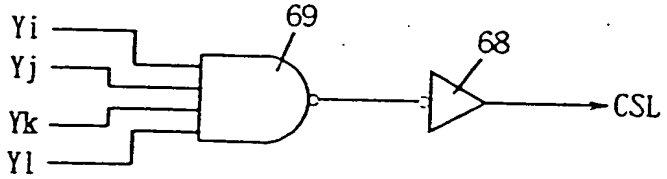


FIG. 51

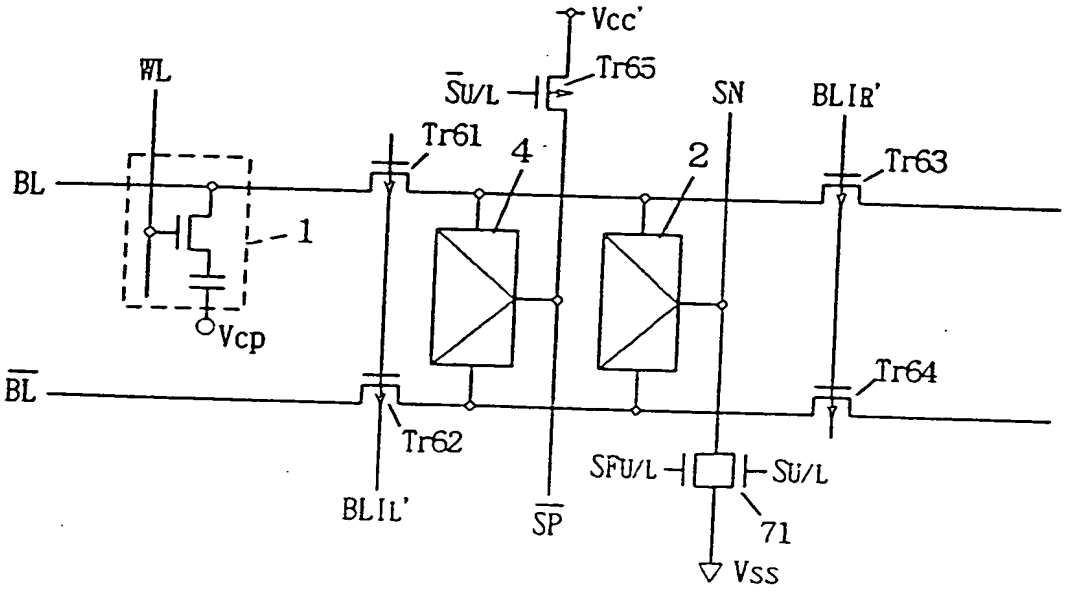

Vcc'
WL
Tr65
SU/L
SN
BLIR'
Tr61
4
2
Tr63
BL
1
Vcp
Tr64
BL
Tr62
SFU/L
SU/L
BLIL'
SP
71
Vss

FIG. 52

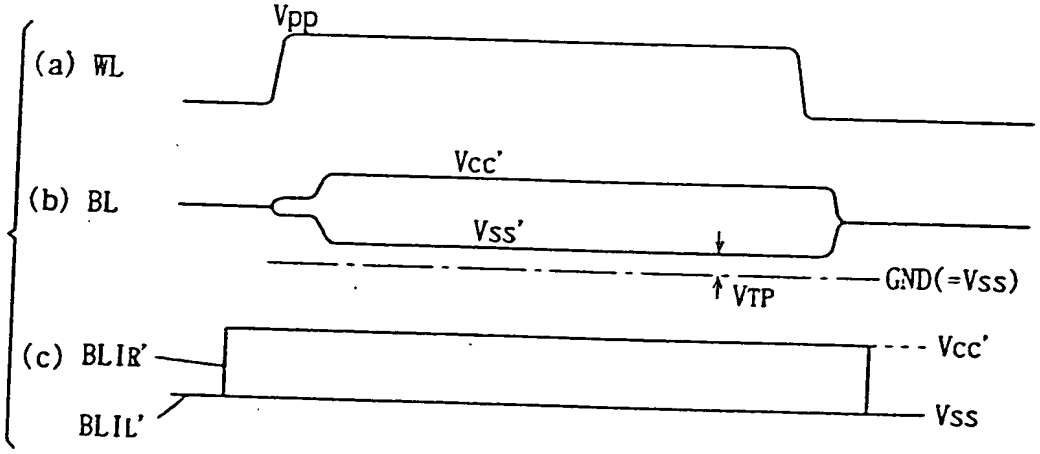

(a) WL
Vpp
(b) BL
Vcc'
Vss'
VTP
GND(=Vss)
(c) BLIR'
BLIL'
Vcc'
Vss

FIG. 53

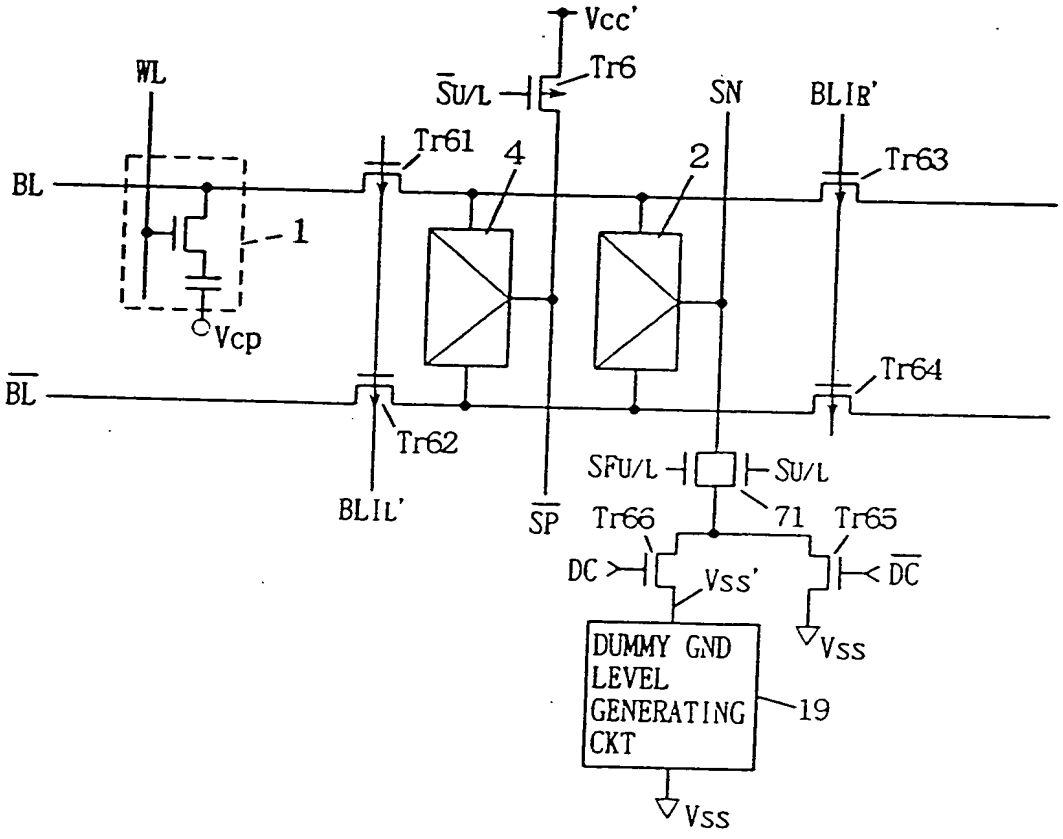

Vcc'
WL
Tr6
SU/L
SN
BLIR'
Tr61
4
2
Tr63
BL
1
Vcp
Tr64
BL
Tr62
SFU/L
SU/L
BLIL'
SP
Tr66
71
Tr65
DC
Vss'
DC
Vss
DUMMY GND LEVEL GENERATING CKT
19
Vss

FIG. 54

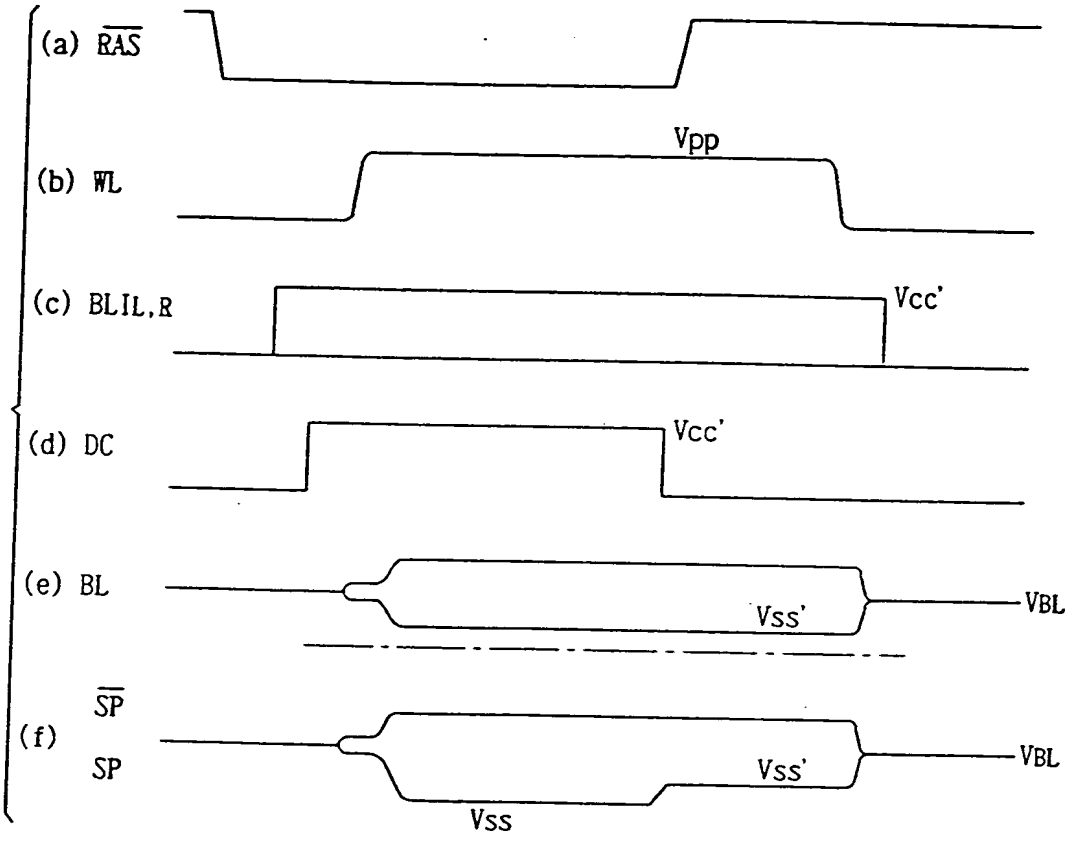

(a) $\overline{RAS}$
(b) WL
Vpp
(c) BLIL,R
Vcc'
(d) DC
Vcc'
(e) BL
Vss'
VBL
(f)
$\overline{SP}$
SP
Vss'
VBL
Vss

FIG. 55

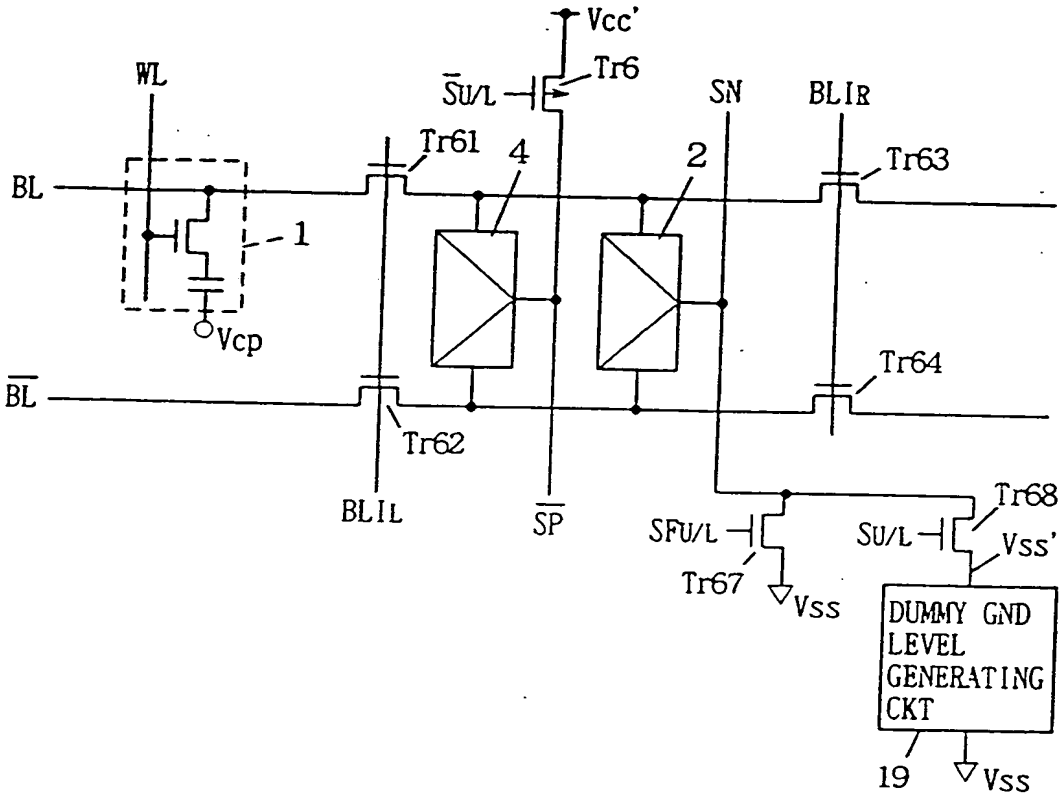

Vcc'
WL
$\overline{SU/L}$
Tr6
SN
BLIR
Tr61
4
2
Tr63
BL
1
Vcp
Tr64
$\overline{BL}$
Tr62
BLIL
$\overline{SP}$
Tr68
SFU/L
SU/L
Vss'
Tr67
Vss
DUMMY GND LEVEL GENERATING CKT
19
Vss

FIG. 56

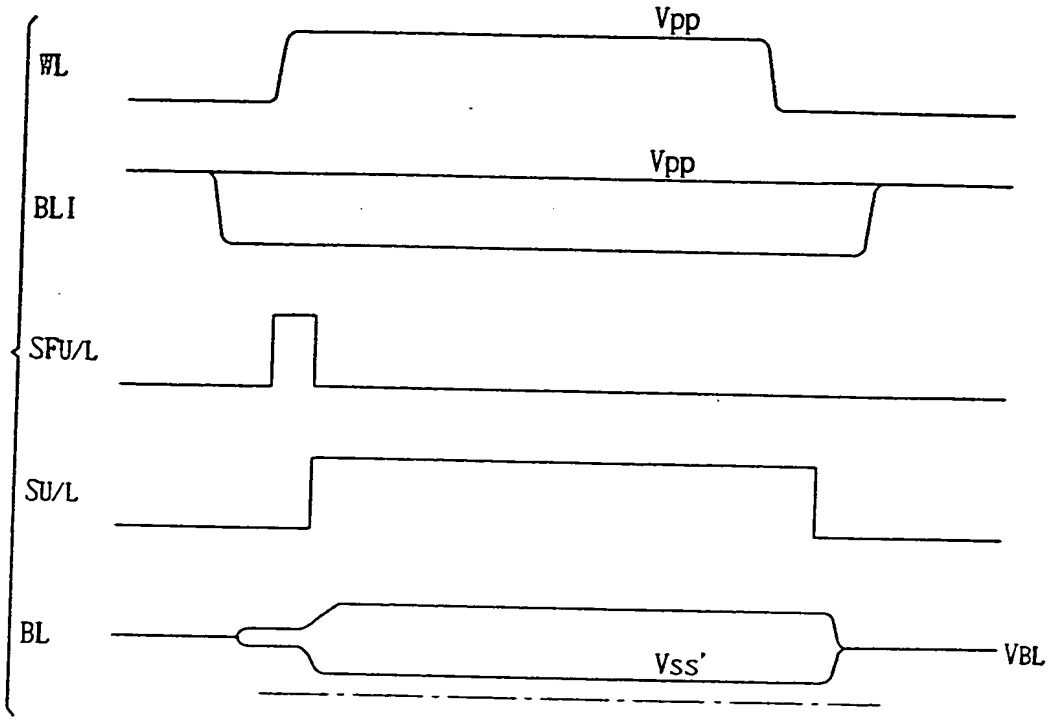

Vpp
WL
Vpp
BLI
SFU/L
SU/L
BL
Vss'
VBL

FIG. 57

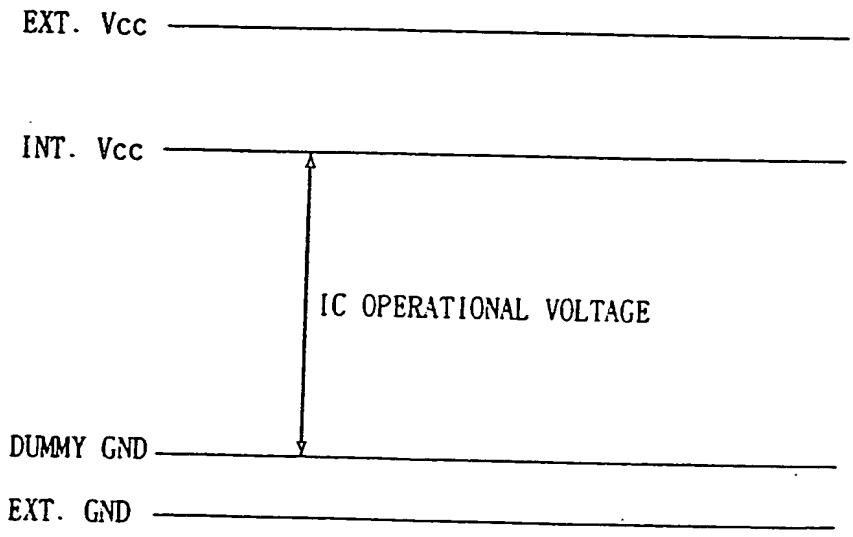

EXT. Vcc
INT. Vcc
IC OPERATIONAL VOLTAGE
DUMMY GND
EXT. GND

FIG. 58

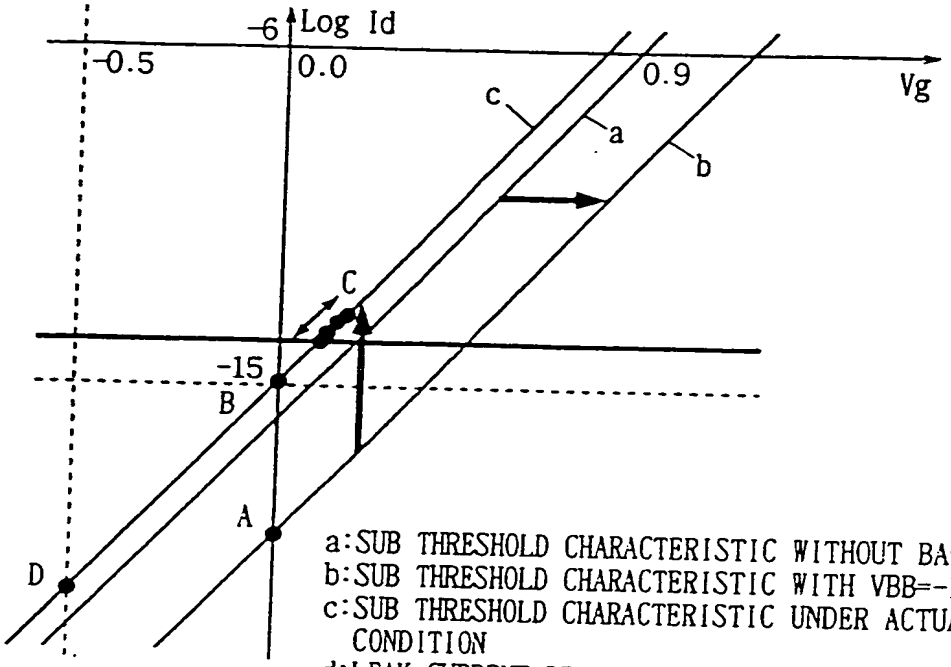

-6
Log Id
-0.5
0.0
0.9
Vg
c
a
b
C
-15
B
A
D
a:SUB THRESHOLD CHARACTERISTIC WITHOUT BACKGATE
b:SUB THRESHOLD CHARACTERISTIC WITH VBB=-1V APPLIED
c:SUB THRESHOLD CHARACTERISTIC UNDER ACTUAL DISTURB CONDITION
d:LEAK CURRENT DETERMINED BY JUNCTION

FIG. 59

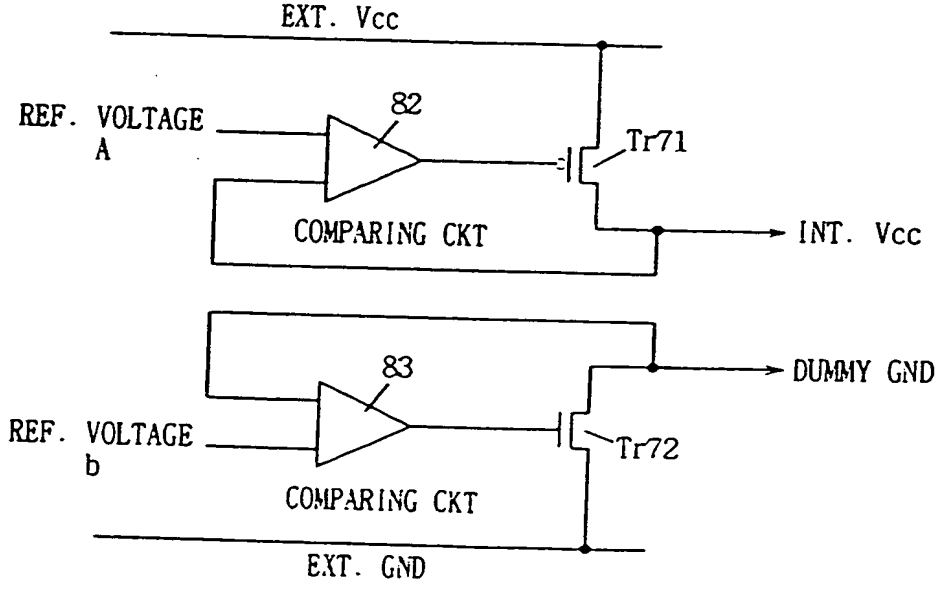

EXT. Vcc
REF. VOLTAGE A
82
Tr71
COMPARING CKT
INT. Vcc
83
DUMMY GND
REF. VOLTAGE b
Tr72
COMPARING CKT
EXT. GND

FIG. 60

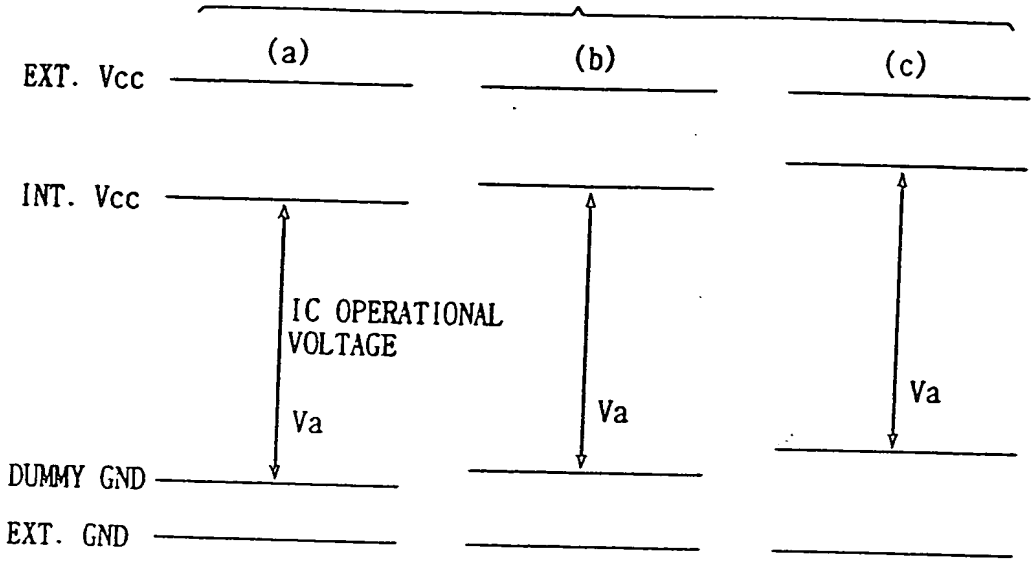

(a)
(b)
(c)
EXT. Vcc
INT. Vcc
IC OPERATIONAL VOLTAGE
Va
Va
Va
DUMMY GND
EXT. GND

FIG. 61

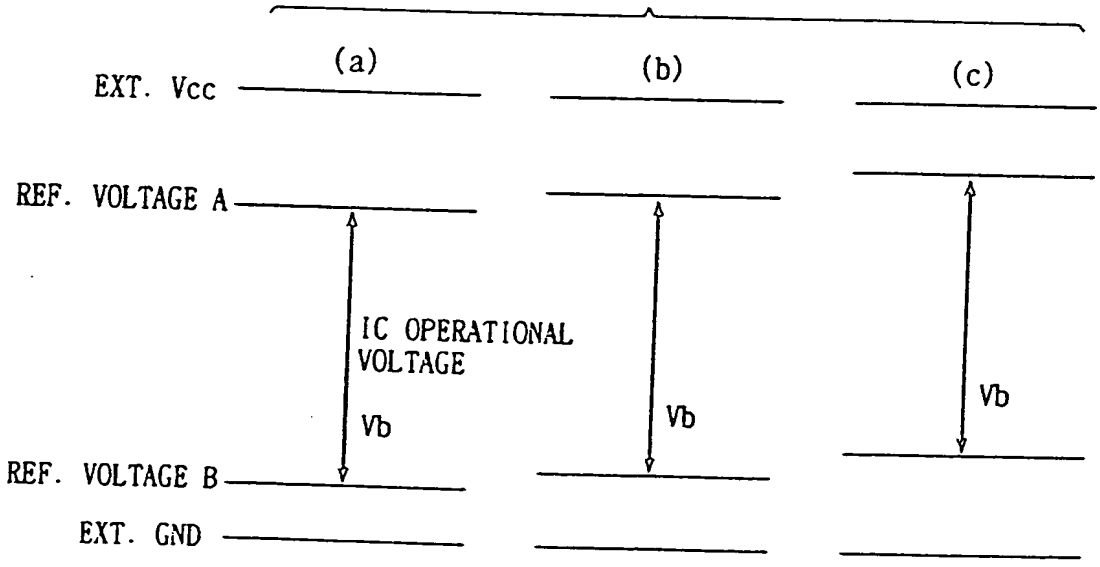
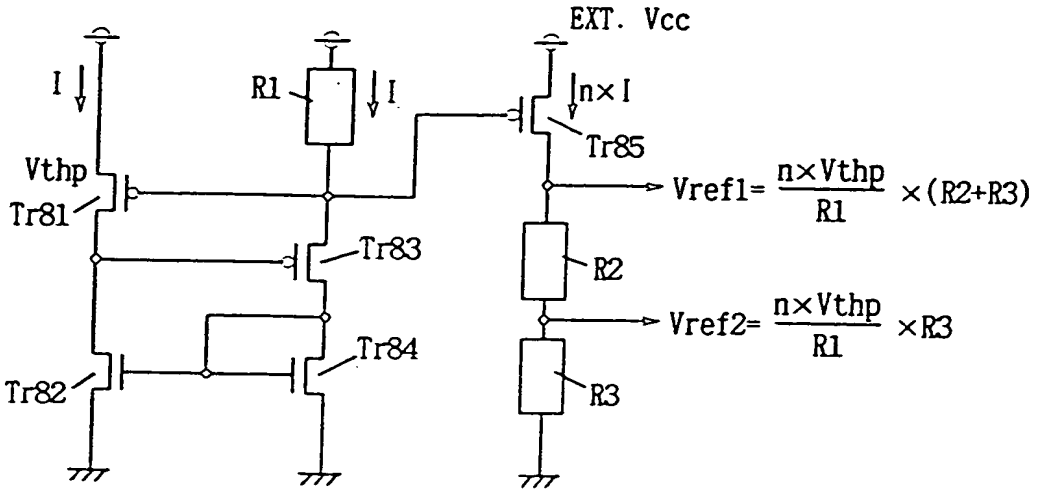

(a)
(b)
(c)
EXT. Vcc
REF. VOLTAGE A
IC OPERATIONAL VOLTAGE
Vb
Vb
Vb
REF. VOLTAGE B
EXT. GND

FIG. 62



$$Vref1 - Vref2 = \frac{n \times Vthp}{R1} \times R2$$

FIG. 63

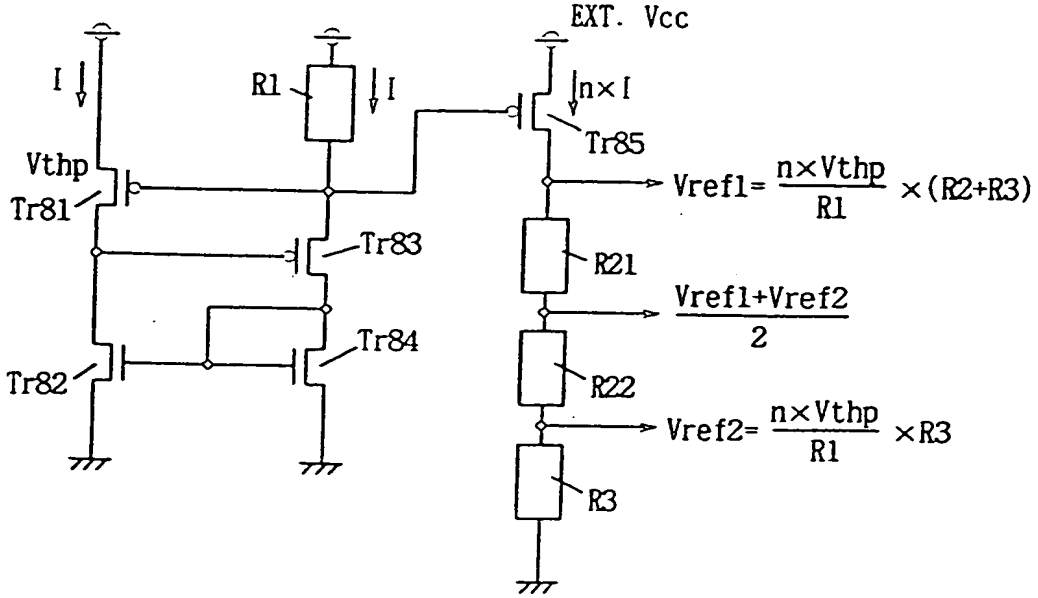


FIG. 64

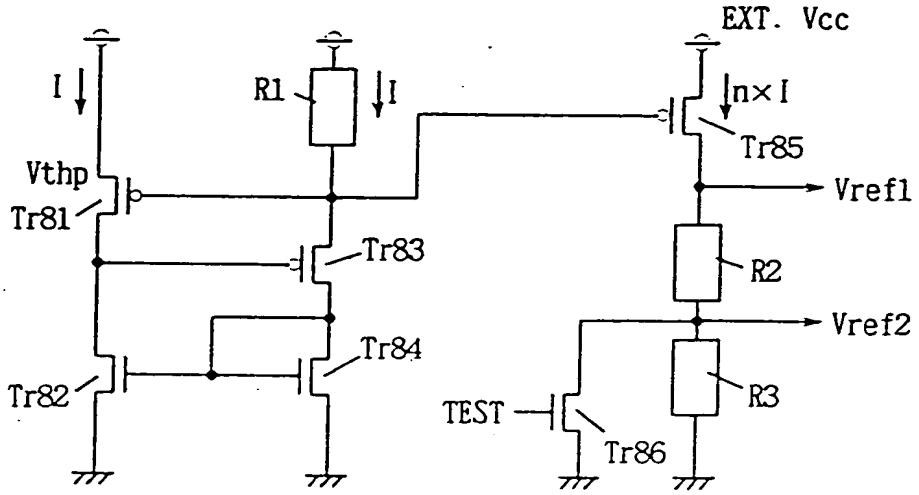

EXT. Vcc
I
R1
I
n×I
Tr85
Vthp
Tr81
Vref1
Tr83
R2
Vref2
Tr84
Tr82
TEST
R3
Tr86

FIG. 65

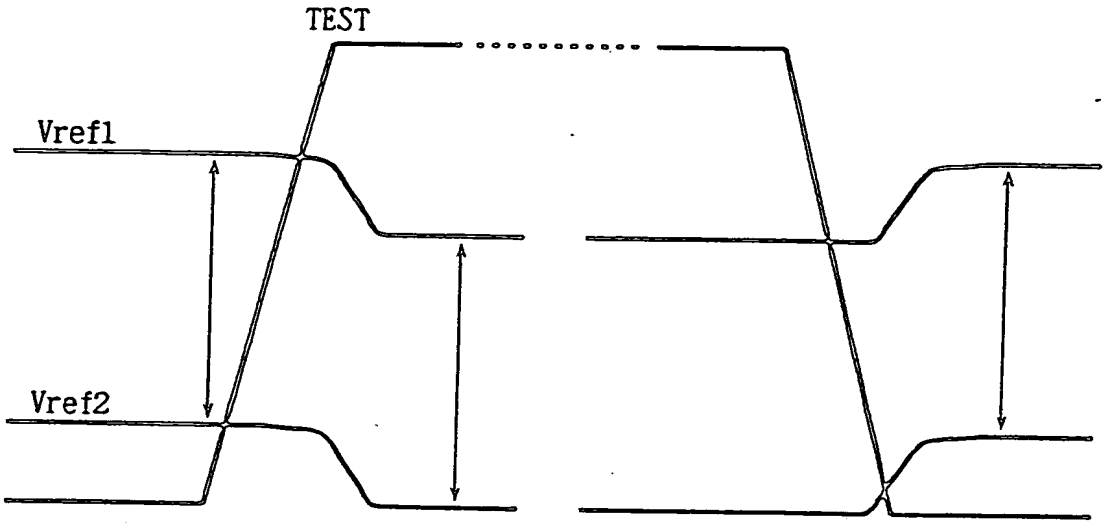

TEST
Vref1
Vref2

FIG. 66

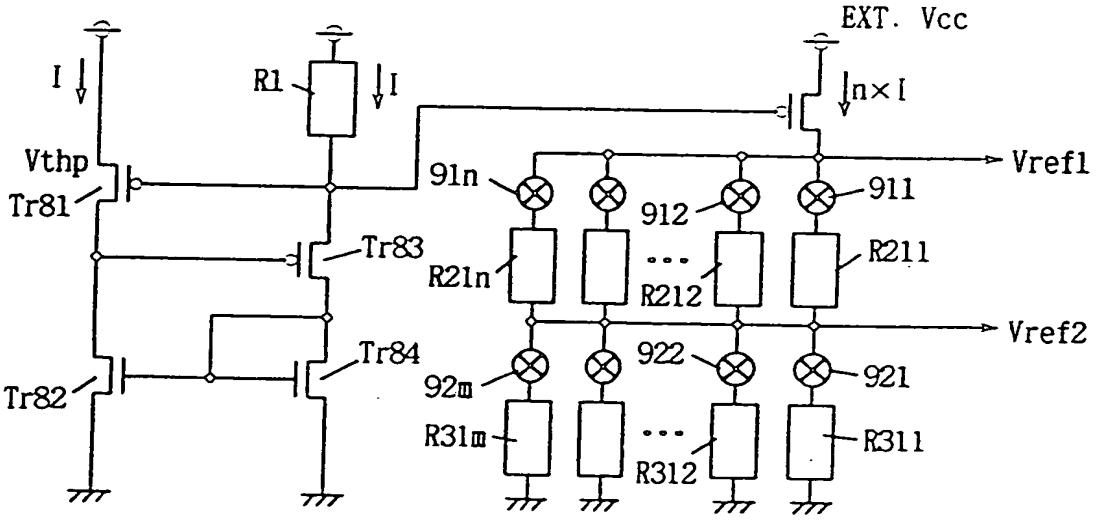

EXT. Vcc
I
R1
I
n×I
Vthp
Tr81
91n
912
911
Vref1
Tr83
R21n
R212
R211
Vref2
Tr84
922
Tr82
92m
921
R31m
R312
R311

FIG. 67

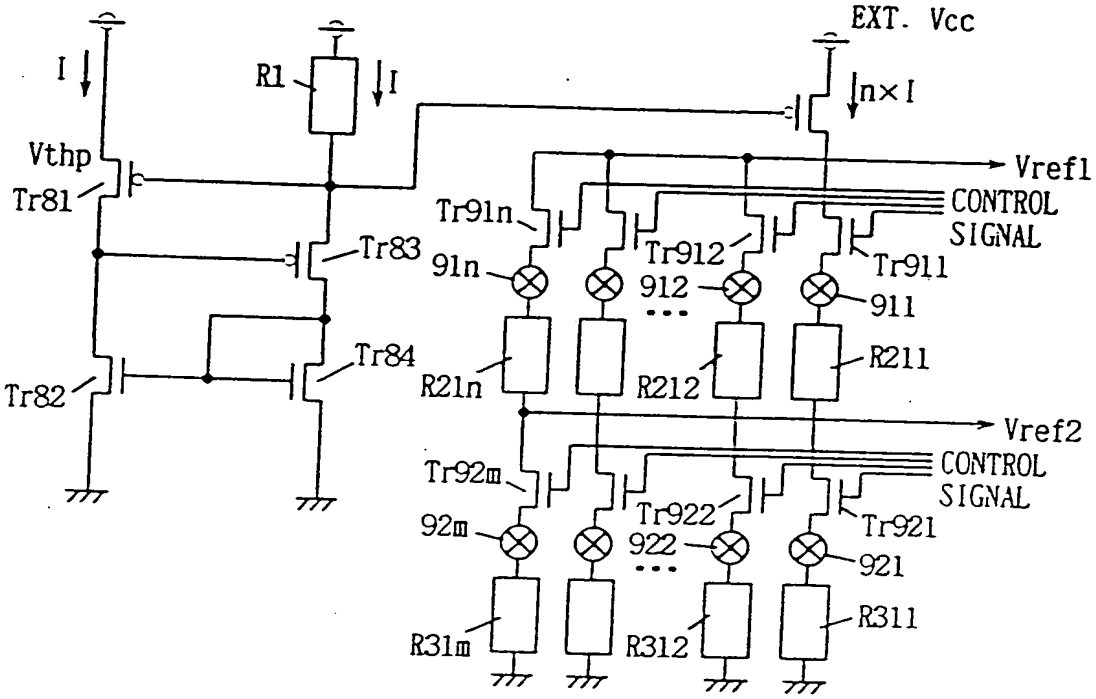

I
R1
I
EXT. Vcc
n×I
Vthp
Tr81
Vref1
CONTROL SIGNAL
Tr91n
Tr912
Tr911
Tr83
91n
912
911
Tr84
Tr82
R21n
R212
R211
Vref2
CONTROL SIGNAL
Tr92m
Tr922
Tr921
92m
922
921
R31m
R312
R311

FIG. 68

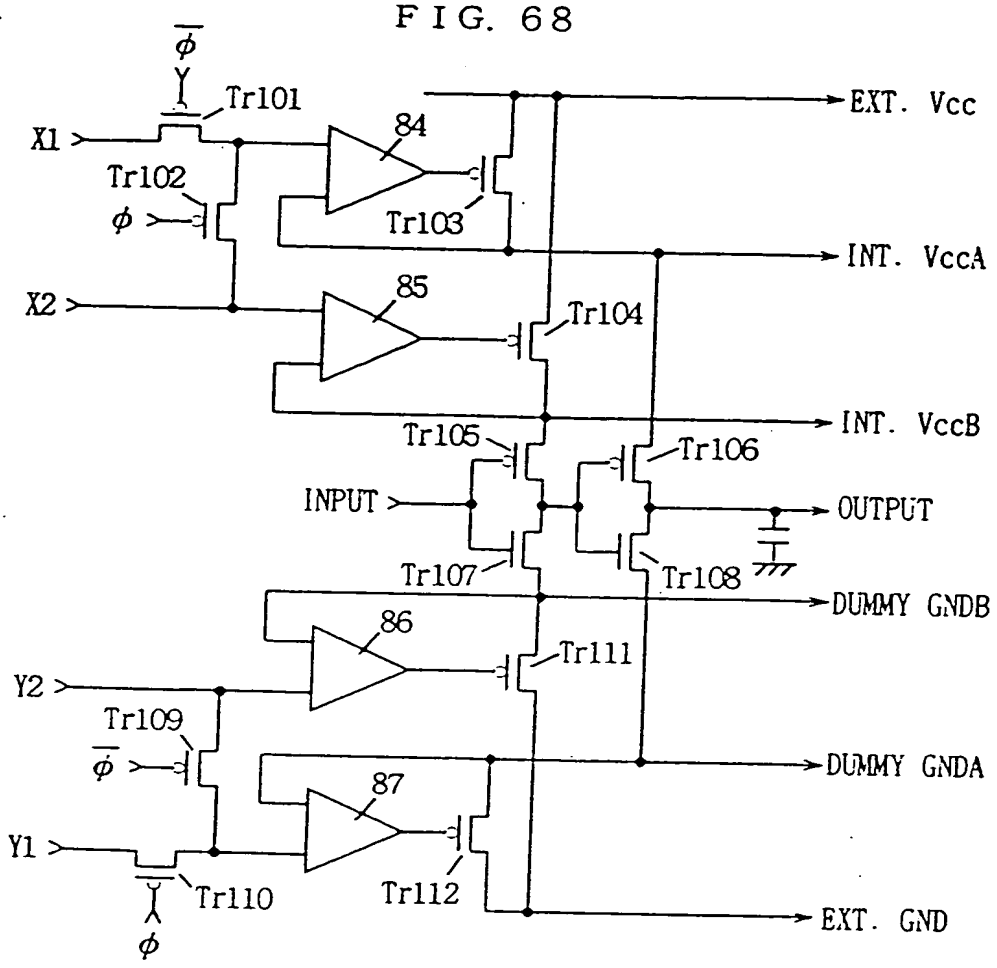

$\overline{\phi}$
Tr101
X1
84
EXT. Vcc
Tr102
ϕ
Tr103
INT. VccA
X2
85
Tr104
INT. VccB
Tr105
Tr106
INPUT
OUTPUT
Tr107
Tr108
DUMMY GNDB
86
Tr111
Y2
Tr109
$\overline{\phi}$
DUMMY GNDA
87
Y1
Tr110
Tr112
ϕ
EXT. GND

FIG. 69

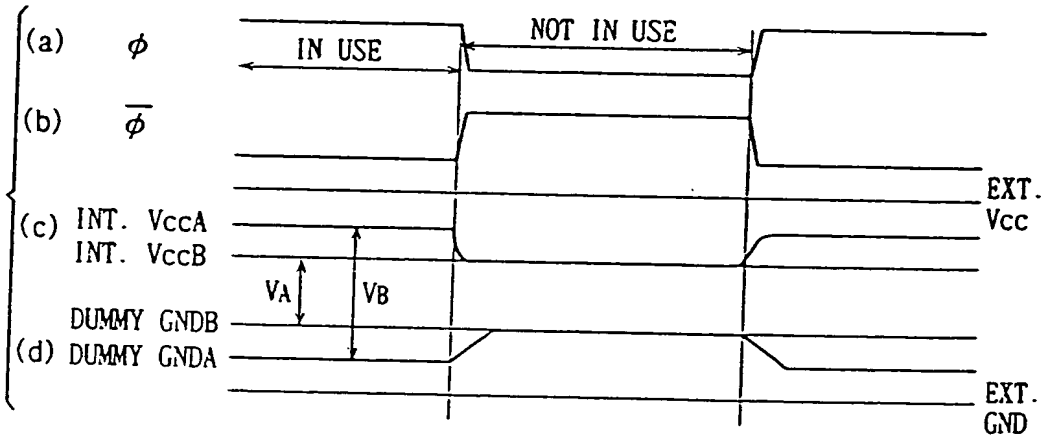

(a) ϕ
(b) $\overline{\phi}$
IN USE
NOT IN USE
(c) INT. VccA
INT. VccB
EXT. Vcc
VA
VB
DUMMY GNDB
(d) DUMMY GNDA
EXT. GND

FIG. 70

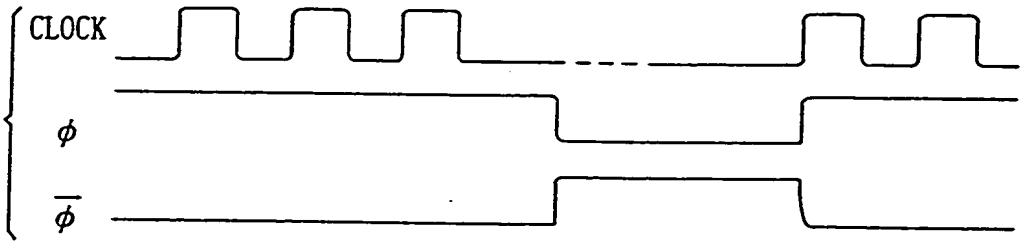


FIG. 71

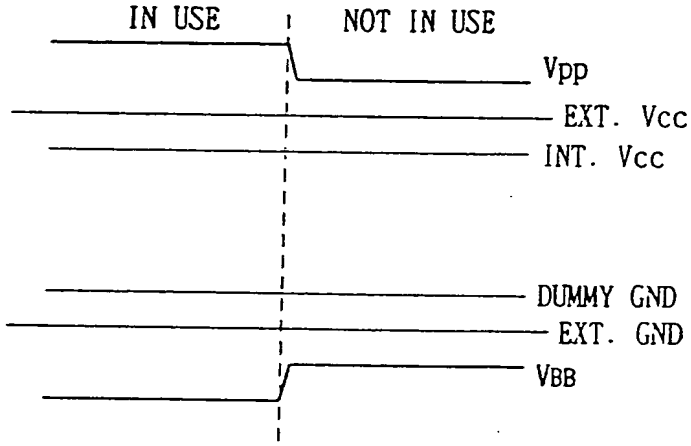


FIG. 72

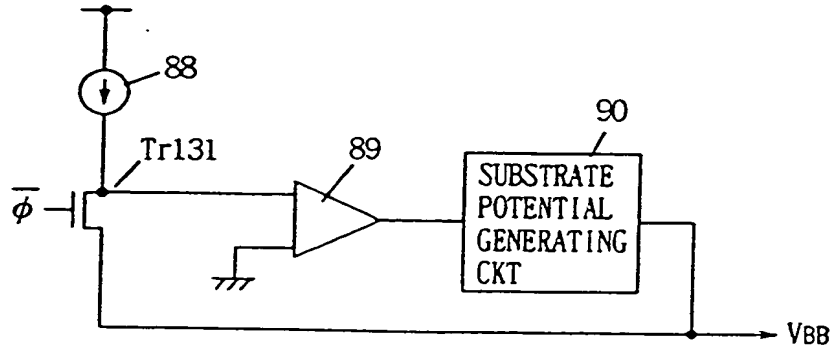


FIG. 73

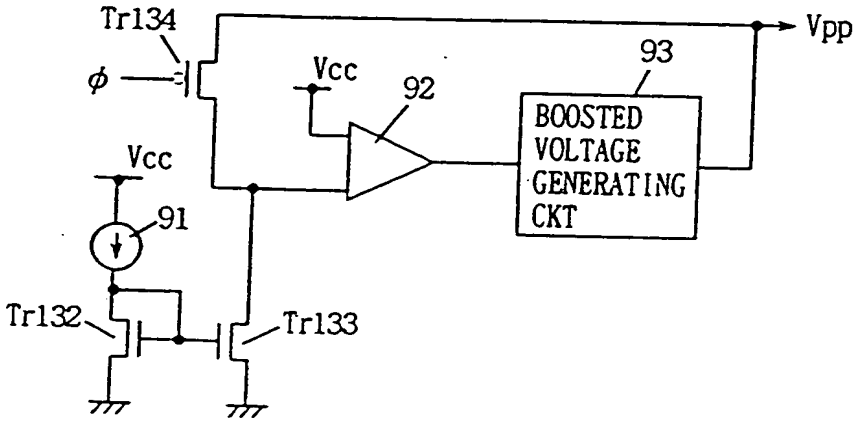

Tr134
Vpp
φ
Vcc
92
93
BOOSTED
VOLTAGE
GENERATING
CKT
Vcc
91
Tr132
Tr133

FIG. 74

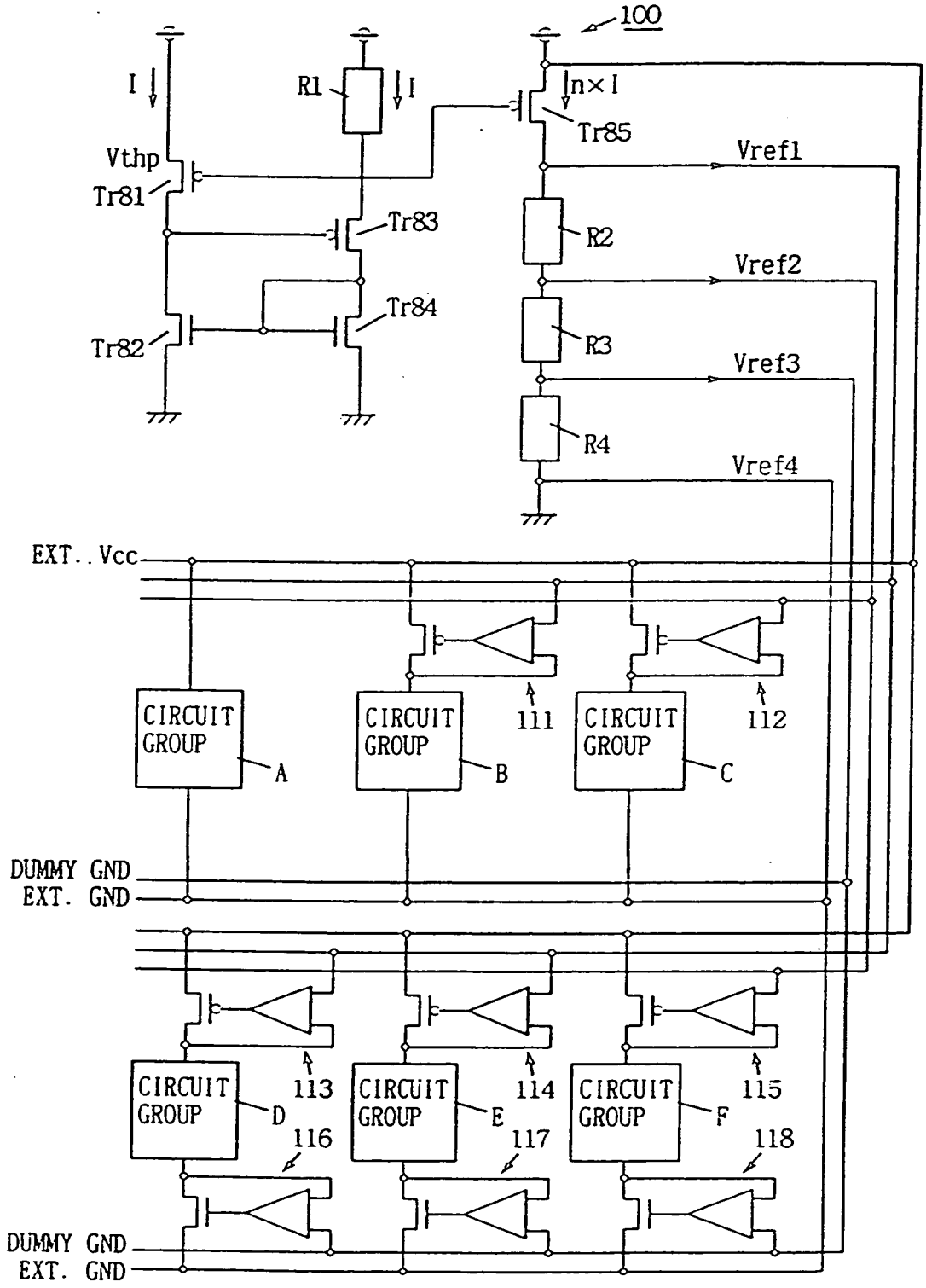

100
I
R1
I
n×I
Tr85
Vthp
Tr81
Vref1
Tr83
R2
Vref2
Tr84
R3
Tr82
Vref3
R4
Vref4
EXT..Vcc
CIRCUIT GROUP A
CIRCUIT GROUP B
111
CIRCUIT GROUP C
112
DUMMY GND
EXT. GND
CIRCUIT GROUP D
113
CIRCUIT GROUP E
114
CIRCUIT GROUP F
115
116
117
118
DUMMY GND
EXT. GND

FIG. 75

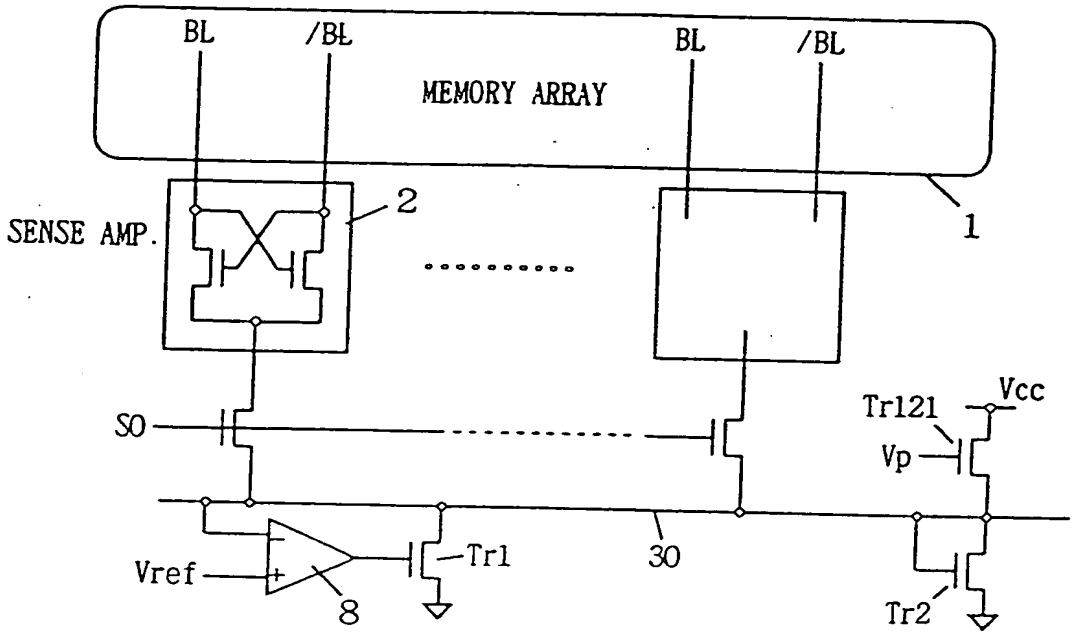

BL
/BL
MEMORY ARRAY
BL
/BL
SENSE AMP.
2
1
SO
Tr121
Vcc
Vp
Vref
8
Tr1
30
Tr2

FIG. 76

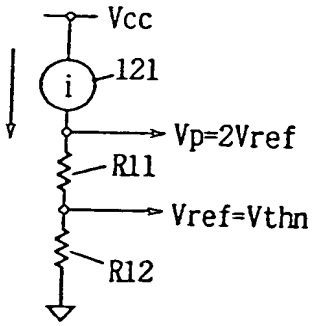

Vcc
i
121
Vp=2Vref
R11
Vref=Vthn
R12

FIG. 77

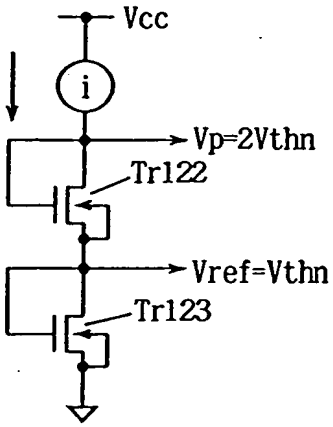


FIG. 78

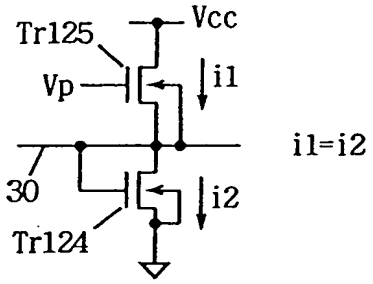


FIG. 79

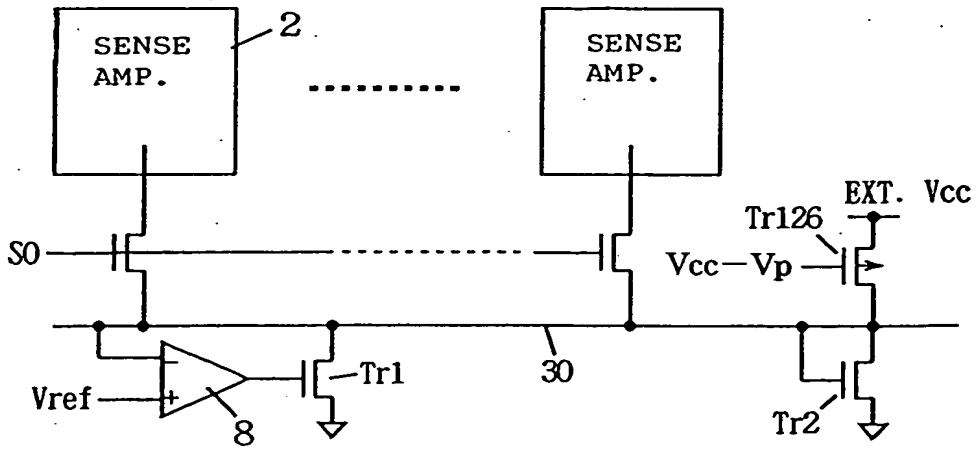


FIG. 80

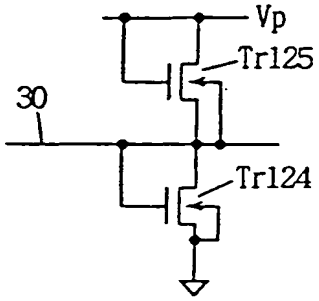


FIG. 81

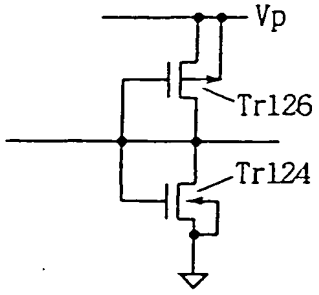


FIG. 82

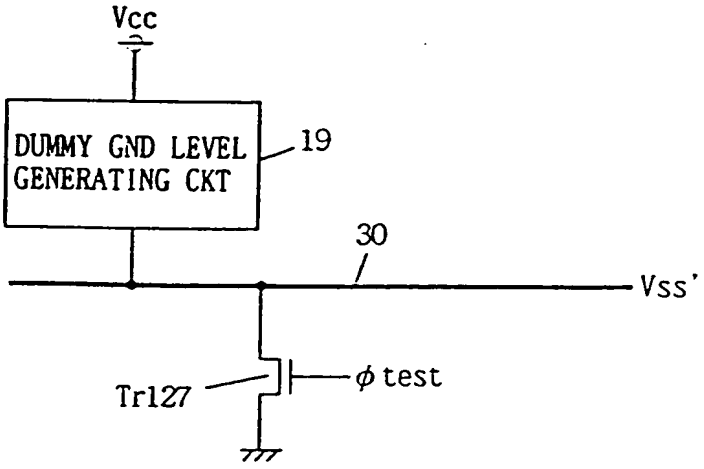


FIG. 83

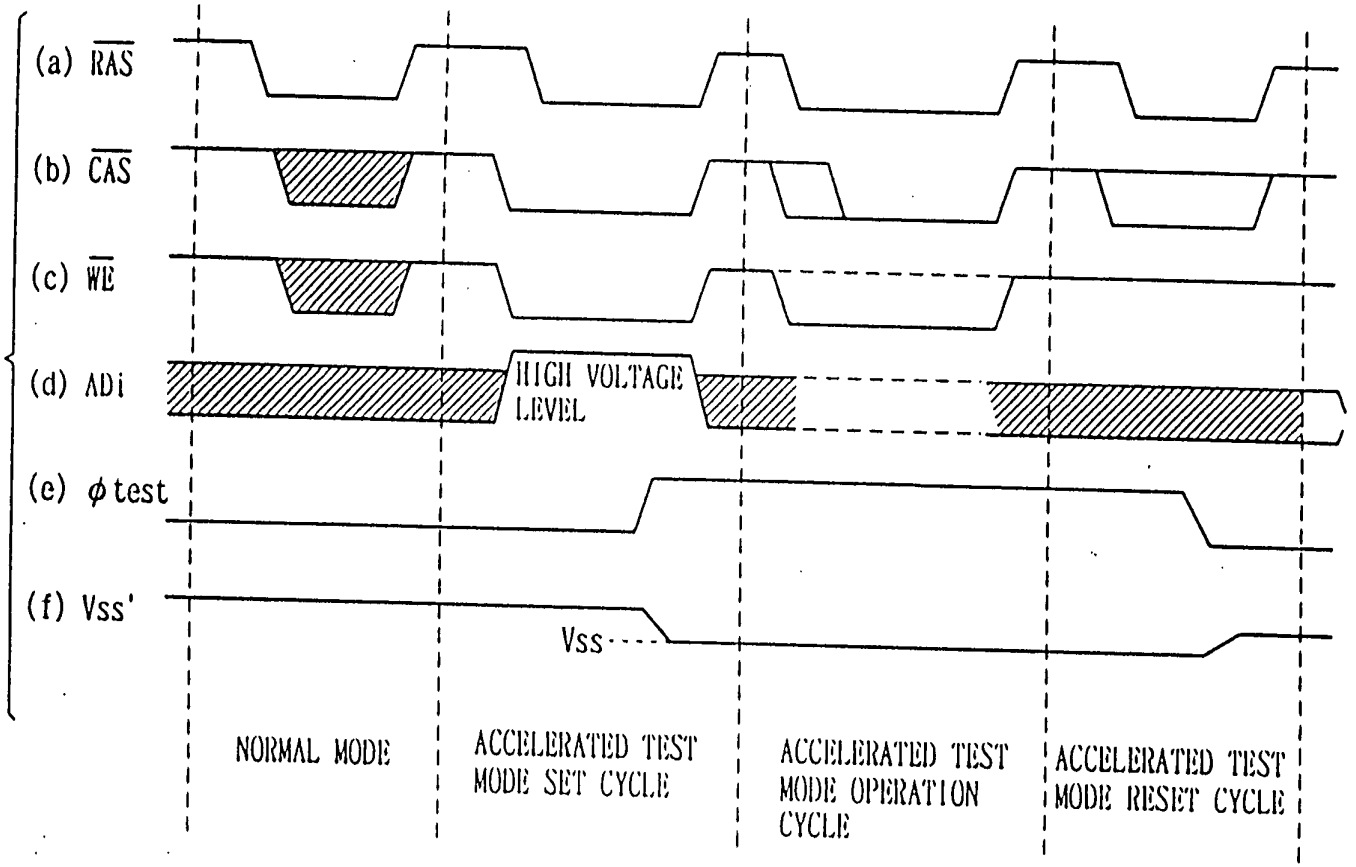

(a) $\overline{RAS}$
(b) $\overline{CAS}$
(c) $\overline{WE}$
(d) ADi
HIGH VOLTAGE LEVEL
(e) ϕ test
(f) Vss'
Vss
NORMAL MODE
ACCELERATED TEST MODE SET CYCLE
ACCELERATED TEST MODE OPERATION CYCLE
ACCELERATED TEST MODE RESET CYCLE

FIG. 84

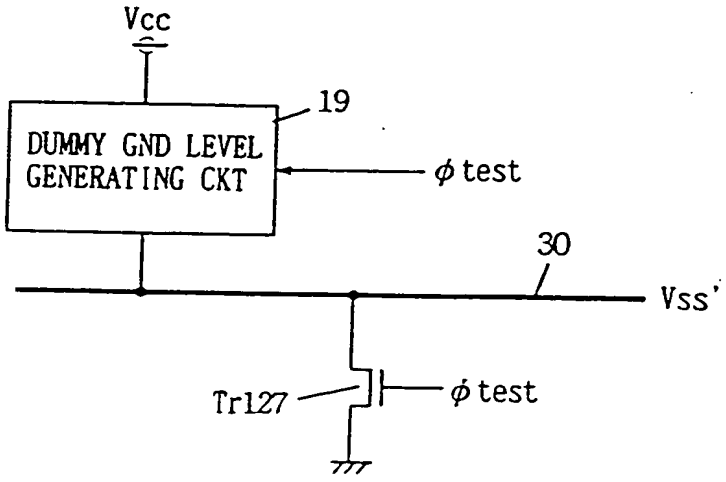

Vcc
19
DUMMY GND LEVEL GENERATING CKT
φ test
30
Vss'
Tr127
φ test

FIG. 85

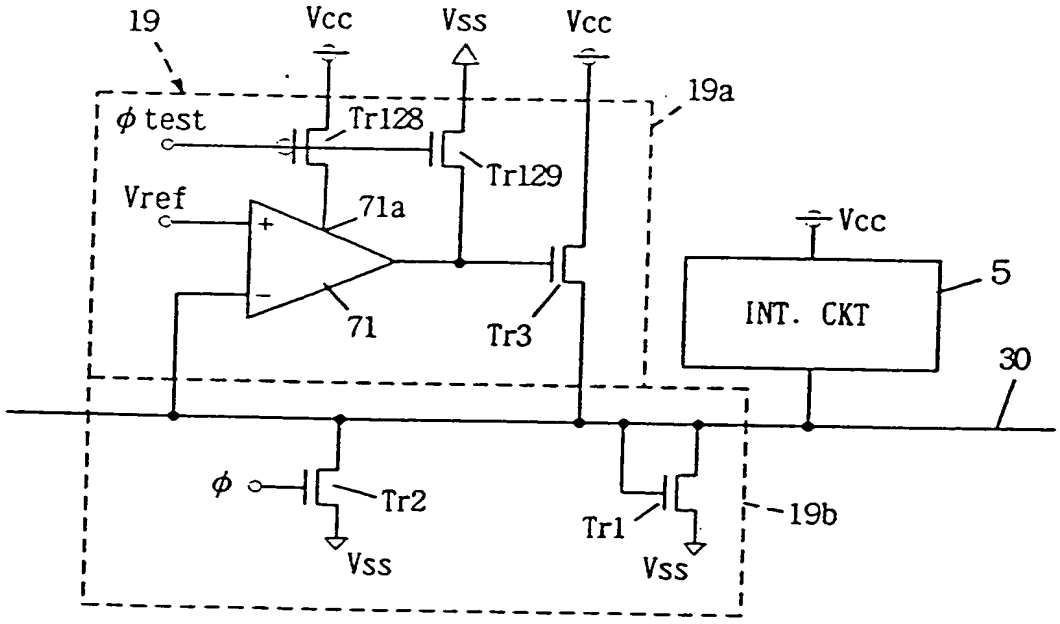

19
Vcc
Vss
Vcc
19a
φ test
Tr128
Tr129
Vref
71a
+
−
71
Tr3
Vcc
INT. CKT
5
30
φ
Tr2
Vss
Tr1
Vss
19b

FIG. 86

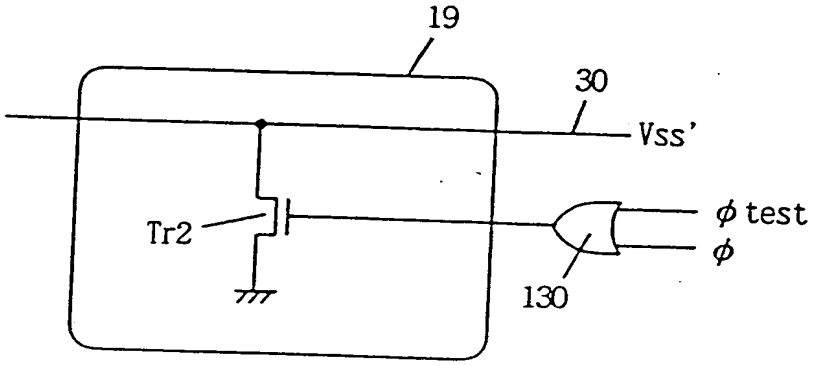


FIG. 87

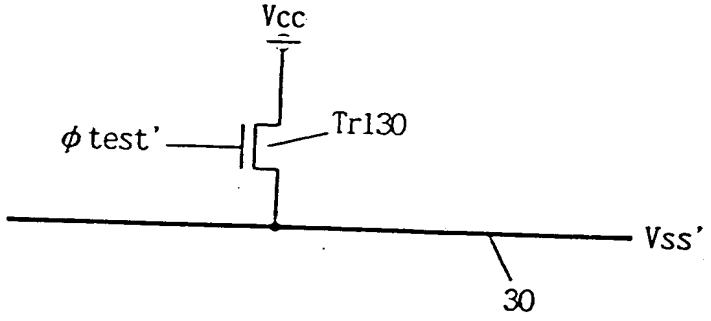


FIG. 88

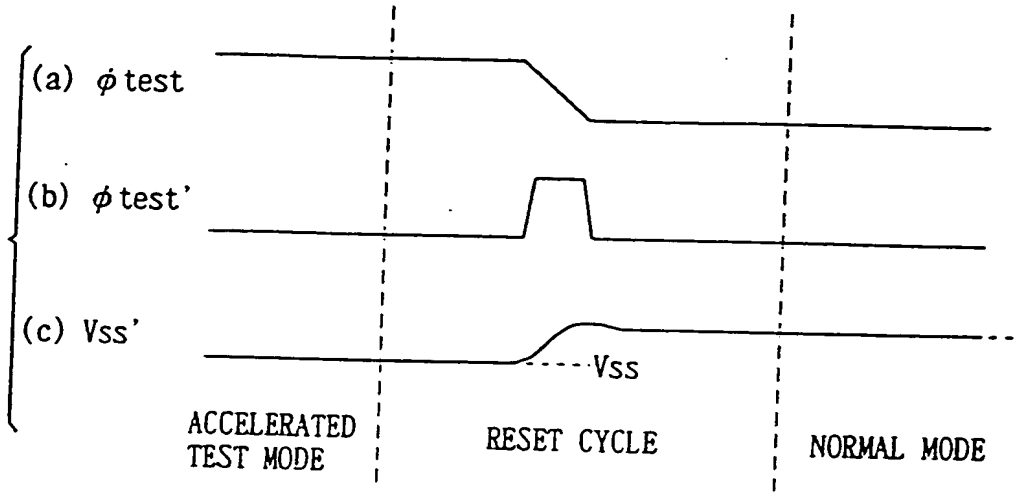


FIG. 89

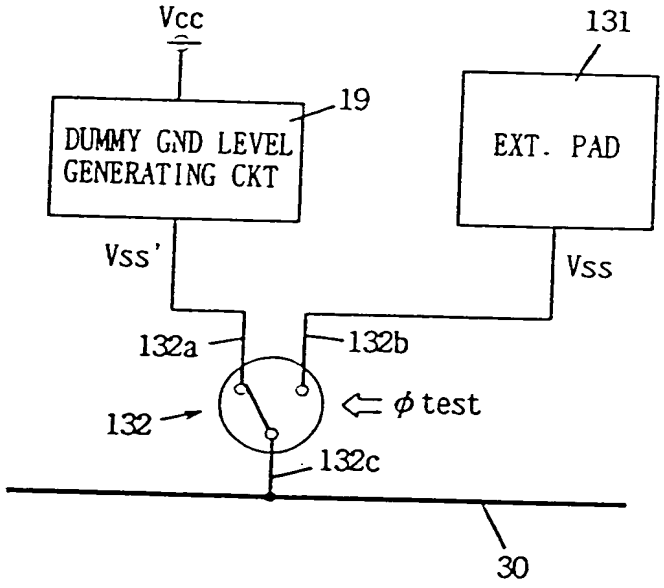


FIG. 90

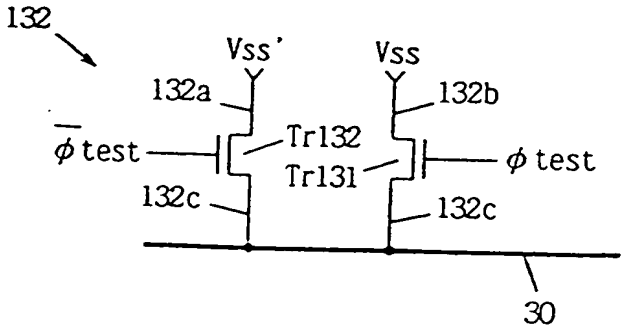


FIG. 91

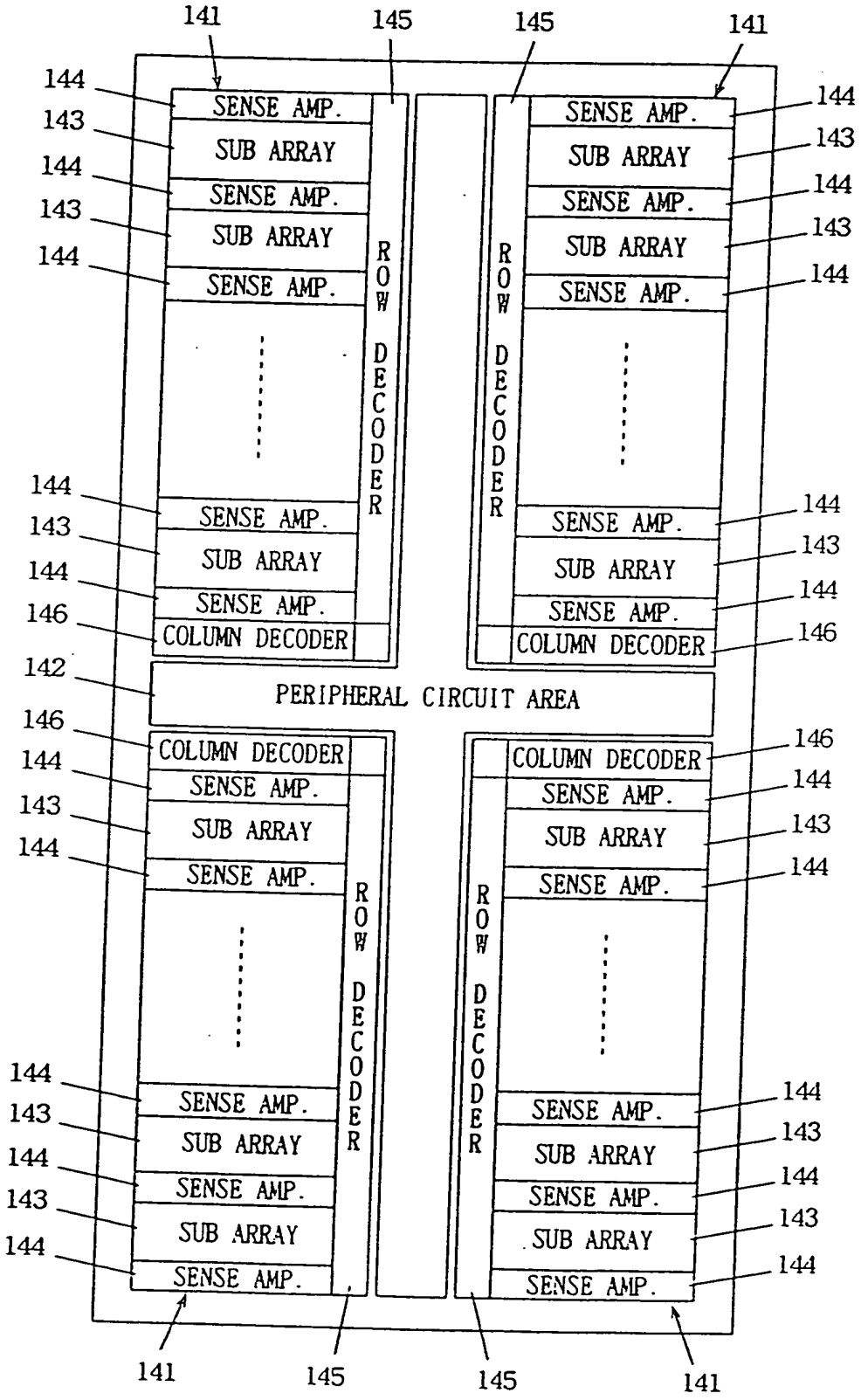

141
145
145
141
144
143
SENSE AMP.
SUB ARRAY
ROW DECODER
COLUMN DECODER
146
142
PERIPHERAL CIRCUIT AREA

FIG. 92

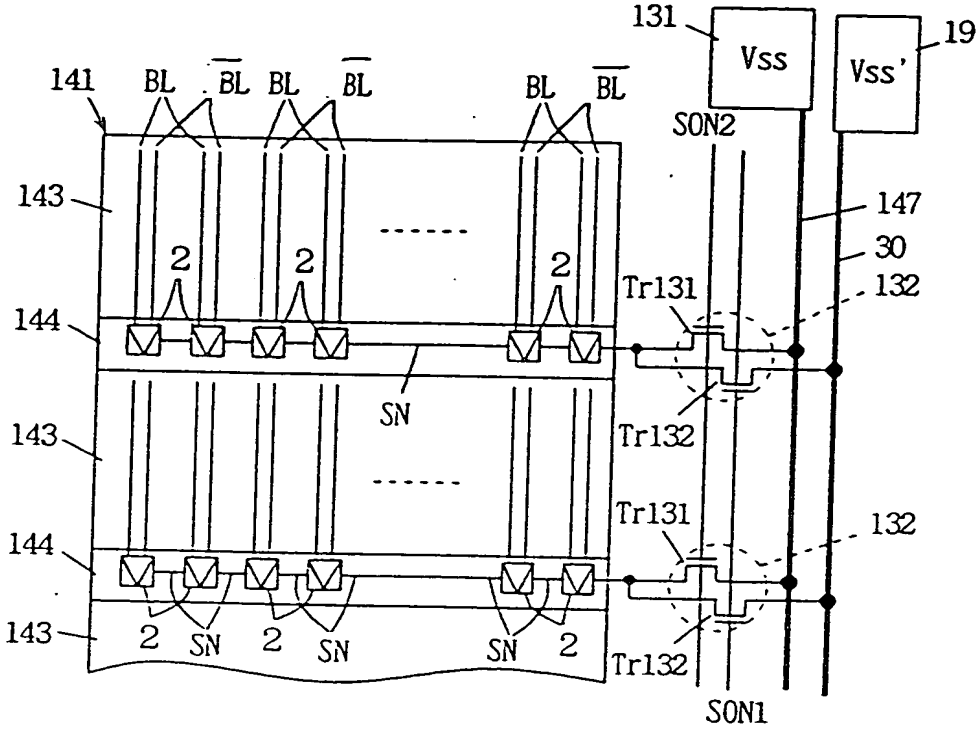


FIG. 93

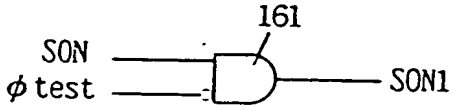


FIG. 94

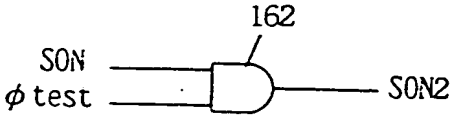


FIG. 95

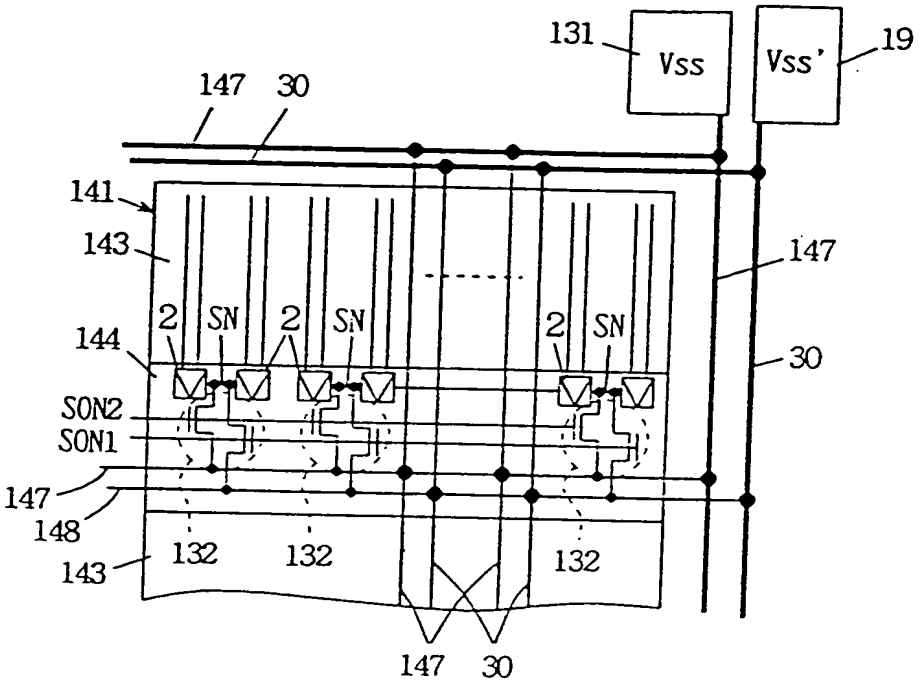

131
Vss
Vss'
19
147
30
141
143
147
2
SN
2
SN
2
SN
144
30
SON2
SON1
147
148
143
132
132
132
147
30

FIG. 96

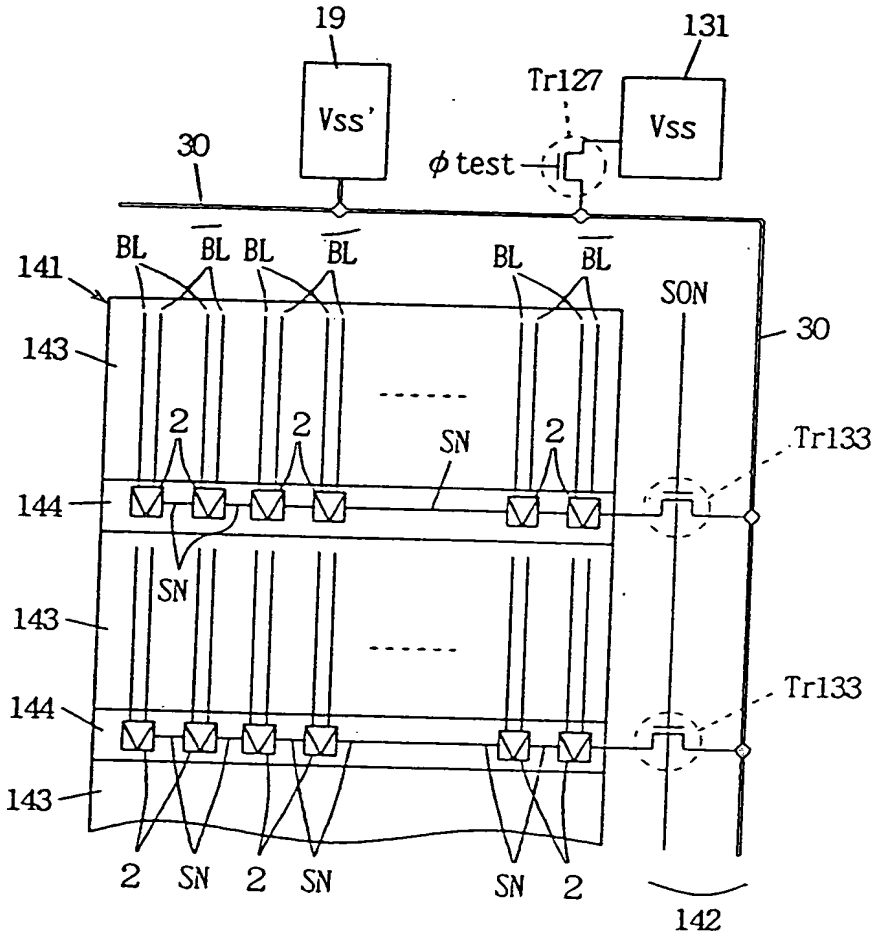

19
131
Tr127
Vss'
Vss
30
φtest
BL
$\overline{BL}$
141
143
144
SON
Tr133
SN
2
142

FIG. 97

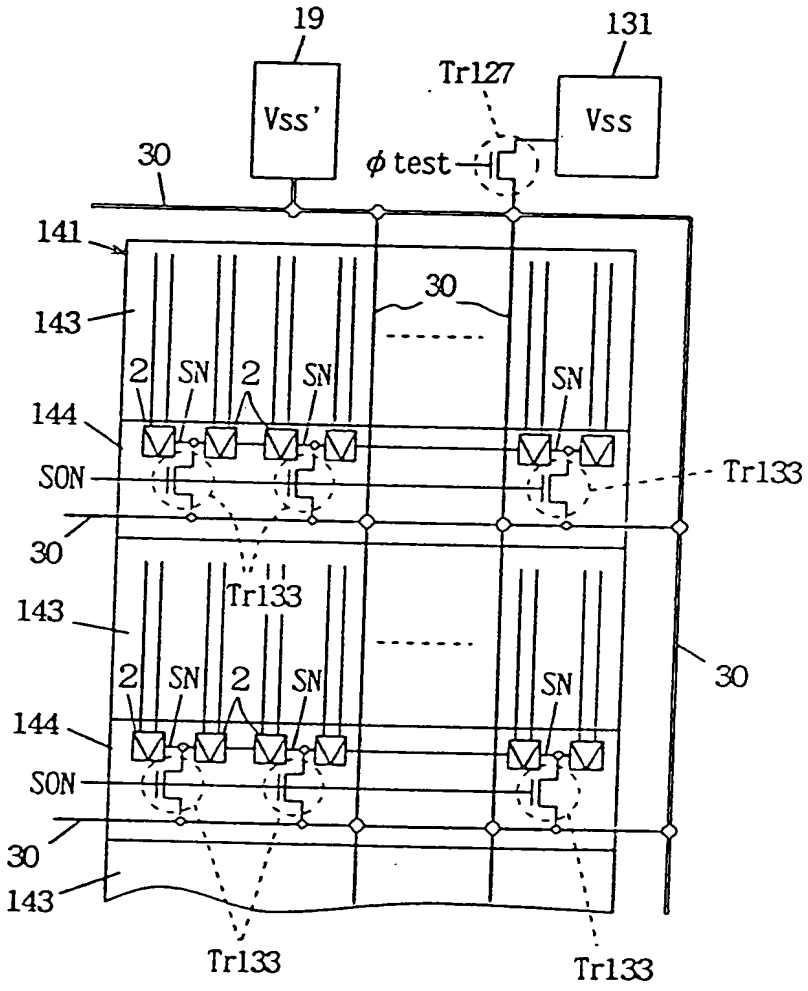

19
131
Tr127
Vss'
Vss
30
φ test
141
143
30
2
SN
2
SN
SN
144
SON
Tr133
30
Tr133
143
30
2
SN
2
SN
SN
144
SON
30
143
Tr133
Tr133

FIG. 98

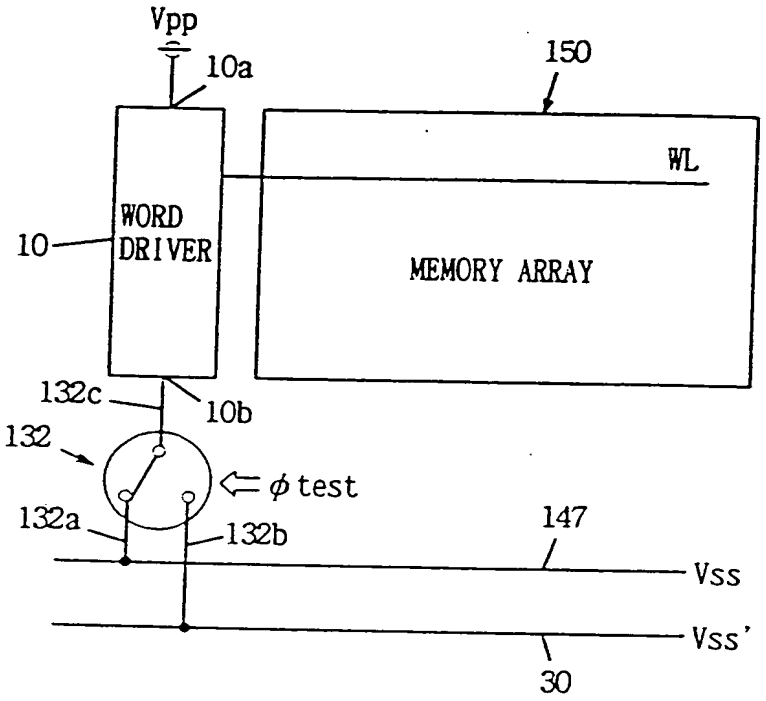

Vpp
10a
150
WL
WORD DRIVER
10
MEMORY ARRAY
132c
10b
132
⇐ φ test
132a
132b
147
Vss
Vss'
30

FIG. 99

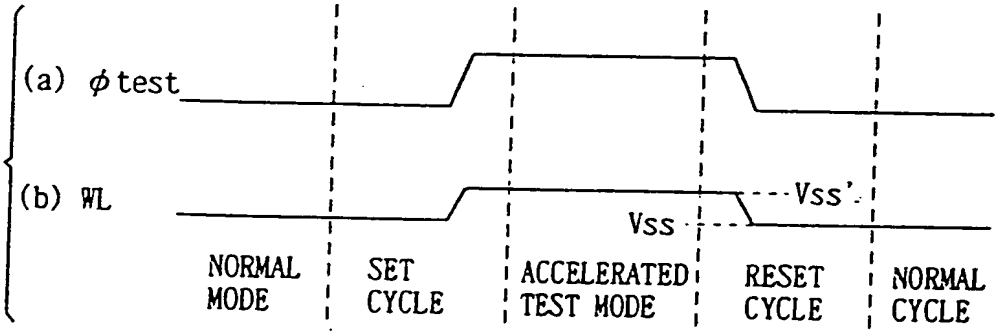

(a) φ test
(b) WL
Vss'
Vss
NORMAL MODE
SET CYCLE
ACCELERATED TEST MODE
RESET CYCLE
NORMAL CYCLE

FIG. 100

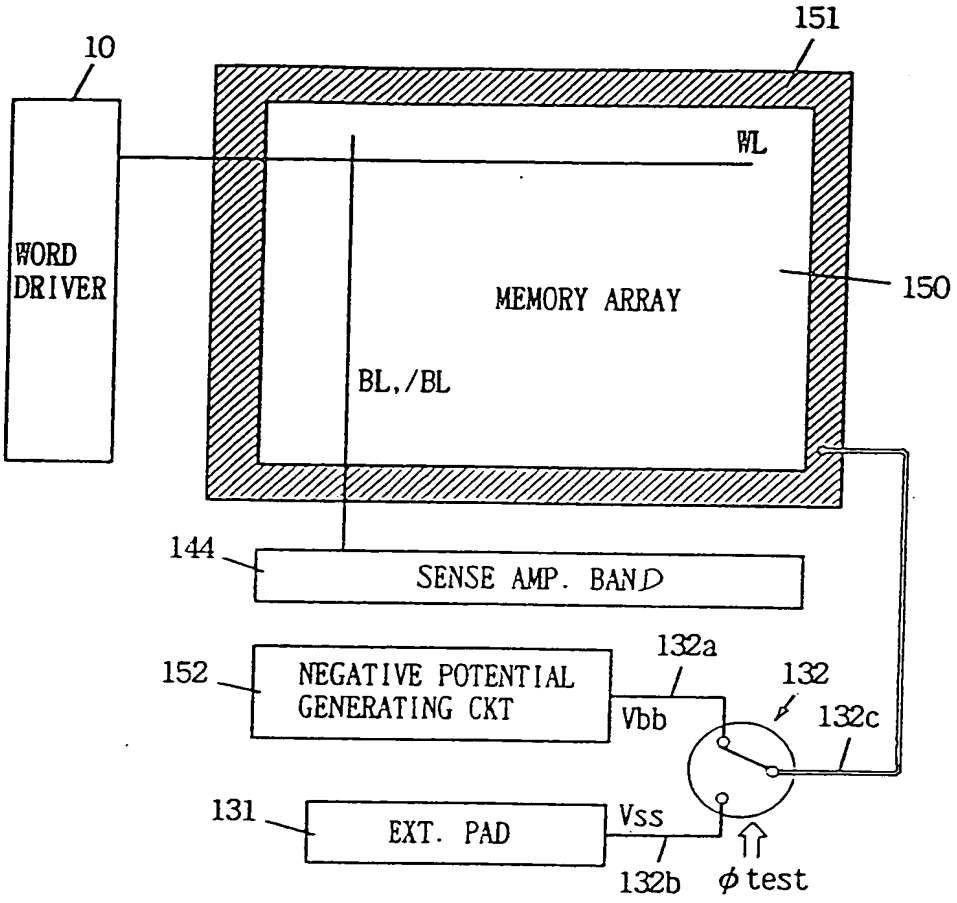
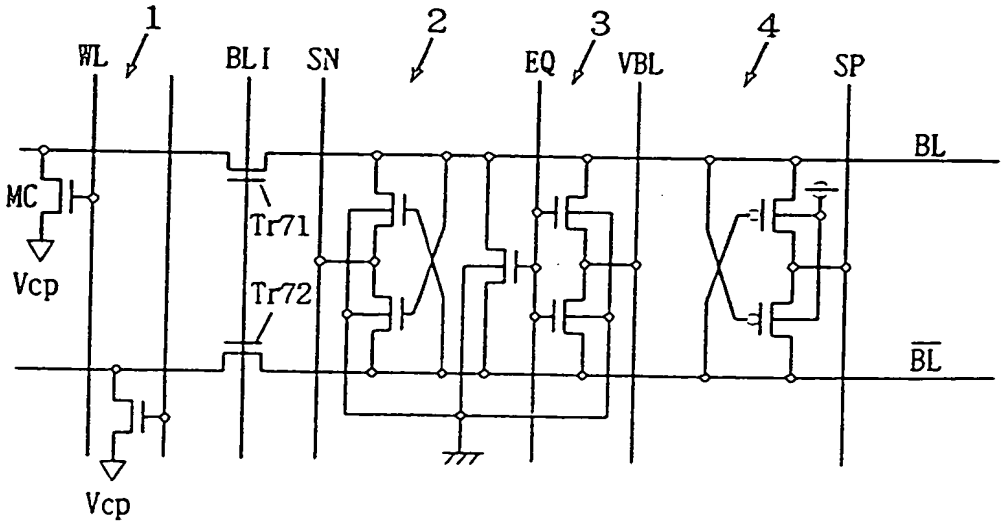


FIG. 101 PRIOR ART



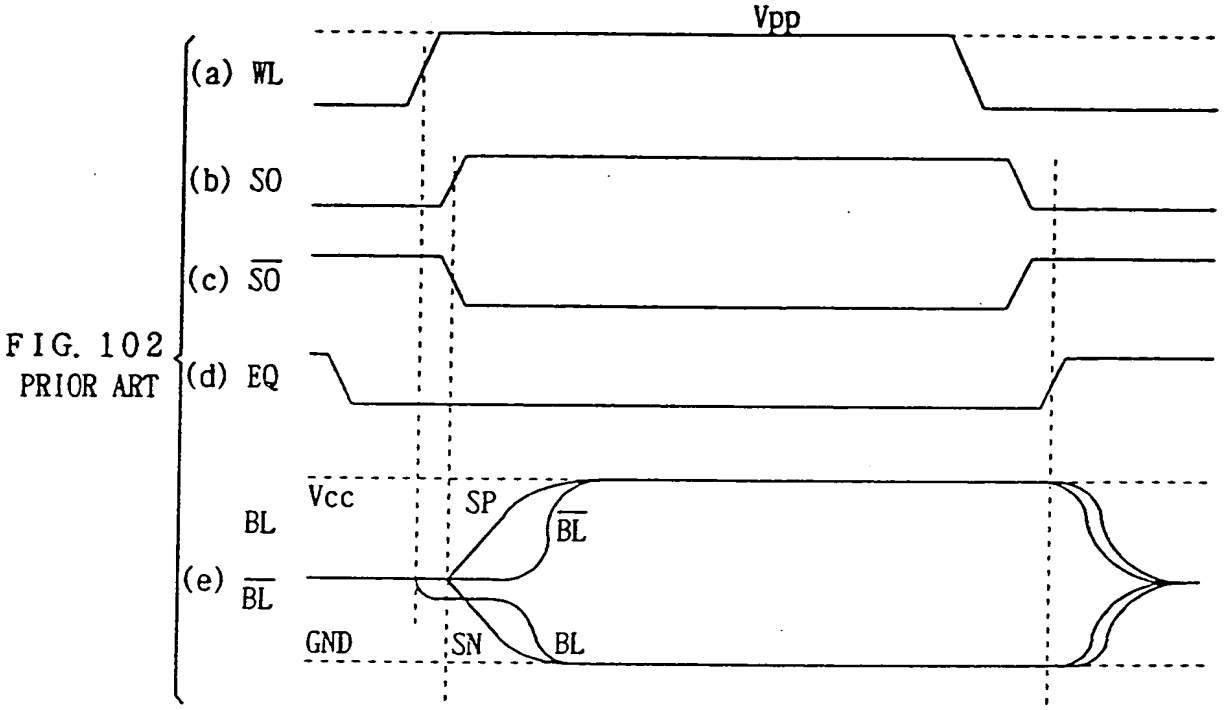


FIG. 102
PRIOR ART